Multi-Gate FD-SOI Single Electron Transistor for hybrid SET-MOSFET quantum computing

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***Abstract*—In this work we explore the fabrication and experimental characterization of multi-gate FD-SOI devices that can operate both as single electron transistors (SETs) and MOSFETs. FD-SOI SET operation is achieved with electrostatically induced tunneling barriers controllable by two barrier gates (B_L and B_R) and a front gate (FG), the device operation being additionally tunable by a bottom gate (BG). Coulomb blockade current measurements at 10 mK and 4 K demonstrate the possibility of a dynamic transition from a FD-SOI MOSFET and SET operation, making this technology suitable for hybrid SET-MOSFET low power cryogenic circuits for quantum information processing. Room temperature back-gate characterization has been performed on ultra-thin film devices proving the effective reduction of charge noise for a specific bias configuration. This experimental work is a step forward towards low noise planar FD-SOI quantum dots based devices with tunable electrostatic control.**

***Index Terms*—SET, FD-SOI, MOSFET, charge noise, cryo-CMOS, quantum computing**

I. Introduction

Silicon-based spin quantum bits (qubits) are promising candidates for the implementation of a quantum processor thanks to the long coherence time of spins and scalability of the technology [1]. Their performance improved considerably over the last few years and great efforts have been made to increase gates fidelity above mK temperatures [2]–[4]. Materials and architecture have been optimized [5] to enable a fast integration of large quantum dots arrays with foundry manufacturing processes [6], [7]. However, with the growth of the number of qubits, integration of control electronics for their manipulation and readout is necessary, posing more stringent limits on power dissipation [8]. Fully depleted silicon-on-insulator (FD-SOI) transistors are known to be best suitable for ultra-low power applications compared to FinFETs [9] and their cryo-characterization has been recently reported [10]. The depletion of majority carriers combined with the threshold tunability through back-gate biasing place them as the optimal candidate for the co-integration of classical and quantum electronics [11].
Single electron transistors (SETs) can be used as charge sensors to read out the spin state of single electrons [12], [13] and their operation can be controlled by integrated CMOS circuits. Some works presented single electron and hole devices fabricated on etched SOI substrates using pattern-dependent-oxidation [14] and silicon nanowires [15]. In this work, we propose for the first time a fully planar multi-gate FD-SOI SET device based on ultra-thin silicon films whose architecture could provide both single electron and hole operation. The device can be dynamically switched to operate as a FD-SOI FET or SET through the activation of tunable tunnel barriers for the ease of integration of FD-SOI qubits with FD-SOI cryo-electronics.

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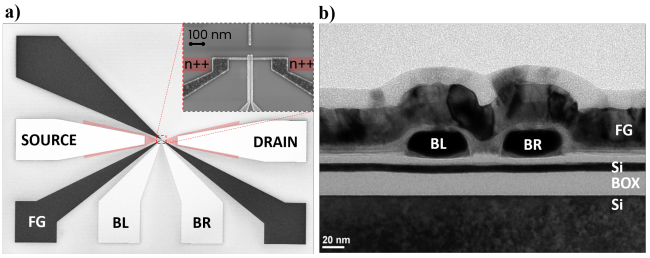

Fig. 1. a) SEM image of a fabricated ultra-thin film (7 nm) planar FD-SOI SET. b) TEM image showing the device cross-section. The same structure was fabricated on a 27 nm SOI substrate.

II. Device fabrication

Our FD-SOI SET device has been taken as a process validation vehicle for the fabrication of fully planar (i.e., without MESA etching and raised contacts) quantum dots devices in ultra-thin silicon films. The layout of the device is shown in fig.1. A single quantum dot is electrostatically defined by two metallic gates arranged along the transistor channel (B_L and B_R) and a single top gate (front gate, F_G). The respective functions of the electrodes are to induce potential tunnel barriers and create inversion layers while tuning the chemical potential of the dot, a similar architecture was presented in [12], [13]. Separated source and drain doped regions give ohmic contacts for electrical conduction.

Two SOI substrates with different top-silicon and buried oxide (BOX) thicknesses have been processed for fabrication. The top silicon layers have been thinned down to 27 nm and

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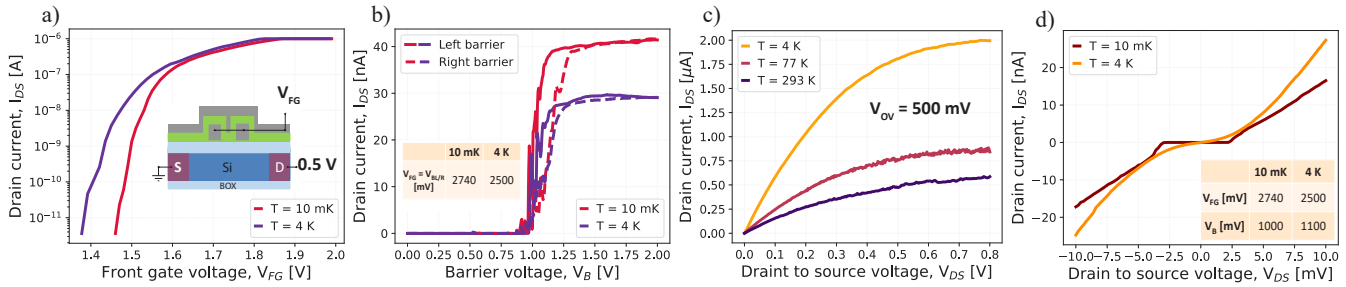

Fig. 2. Cryogenic characterization of a thin-film SET device. a) Transfer characteristic for the common top gate configuration illustrated in the inset (Al_2O_3 in green and Pd gates in grey). b) Transfer characteristic of the left and right barrier gates; a small mismatch of the pinch-off voltage was measured in the device. c) $I_{DS}(V_{DS})$ characteristics at different temperatures for a constant overdrive voltage in the common top gate configuration. d) Zoom-in of the $I_{DS}(V_{DS})$ characteristic around V_{DS}= 0 V. For certain V_{FG} and V_B voltages a no-conduction window was measured due to Coulomb blockade.

7 nm through a few cycles of thermal dry-oxidation and wet-etching (BHF 7:1) to get fully-depleted thin and ultra-thin films. In both samples, the silicon layer was p-type with a room temperature resistivity of 10 Ω·cm, the estimated boron concentration is therefore 10^{15} cm^{-3}. The BOX thickness was 2 μm for the thin-film sample and 20 nm for the ultra-thin film one.

Past works proved that charge noise in MOS-quantum dots is mainly due to impurities in the oxides and at the Si/SiO_2 interfaces [16]. We therefore analyzed the density of charge traps in thermal gate oxides grown with different conditions through C-V characterization of MOS capacitors. A shift of the C-V curves towards ideal values was measured when performing Si dry oxidation in dichloroethane followed by rapid thermal annealing (RTA) at 300°C in forming gas. A gate oxide of 5 nm was grown with the same recipe. The estimated density of charge traps was $N_{eff} \approx 10^{10}\, cm^{-2}$.

The source and drain contact regions have been implanted with phosphorus ions through Plasma Immersion Ion Implantation (PIII) with an energy of 1 keV and a dose ranging from $5 \cdot 10^{15}$ cm^{-2} to $1.1 \cdot 10^{16}$ cm^{-2}. Protections for bond-pads were patterned with a positive electron-beam (e-beam) resist (HSQ). A thick field oxide (Al_2O_3, 20 nm) was deposited through atomic layer deposition (ALD) and selectively etched on the active areas with H_3PO_4 50% at 60°C. Ti/Pt contacts were patterned with standard laser lithography using LOR5A/AZ1512 photoresists, e-beam evaporation and lift-off.

All gate electrodes were patterned with single layer (PMMA950K) e-beam lithography, Ti/Pd evaporation and lift-off. The lowest e-beam dose able to resolve the mininum features size (30 nm) was selected to not damage the BOX of the SOI chips and a source-to-sample working distance of 1010 mm was used during evaporation to facilitate the lift-off. The choice of materials was mainly dictated by the ease of nanofabrication, it is indeed known that Pd has a smaller grain size compared to Al and reduced mismatch of thermal expansion coefficient to that of Si [5]. A negligible line edge roughness was measured in all the analyzed devices after lift-off. 5 nm of Al_2O_3 were deposited through ALD for a proper insulation of the two metallic layers and a RTA step was performed in forming gas at 300°C after each deposition.

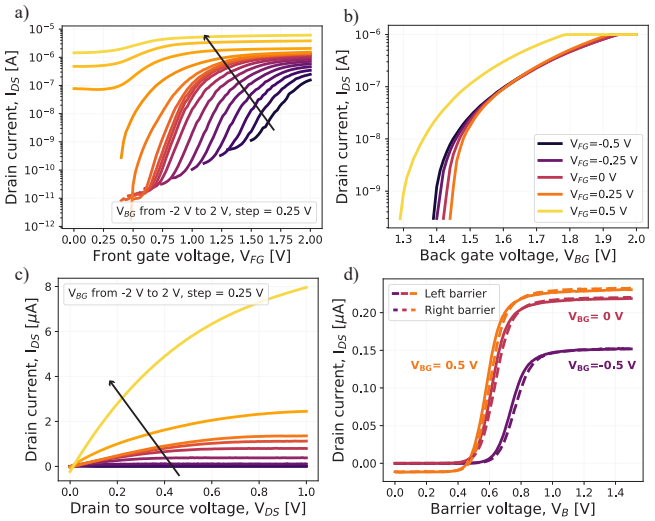

Fig. 3. Room temperature characterization of ultra-thin FD-SOI SET. a) Common top gate transfer characteristics $I_{DS}(V_{FG})$ for different back-gate voltages ($V_{FG} = V_B$, $V_{DS} = 0.5$ V). b) Back gate transfer characteristics $I_{DS}(V_{FG})$ for different front-gate voltages (V_{DS} = 500 mV). c) $I_{DS}(V_{DS})$ characteristics measured at V_{FG} = 1.5 V for different back-gate voltages. d) $I_{DS}(V_B)$ for left and right barrier gates ($V_{FG} = V_{B1/2}$ = 1.5 V, V_{DS} = 100 mV).

Finally, a thick Al_2O_3 capping layer was deposited and wet-etched for the re-opening of contacts prior to wire bonding.

III. Results

Room temperature electrical characterizations were performed with a Keithley 4200A-SCS parameter analyzer and DC cryo-measurements were taken in a LD Bluefors dilution refrigerator. We focused our analysis on the FET and SET characteristics and tested the back-gate control at room temperature on the ultra-thin film sample.

A. Front and back gated MOSFET characteristics

Transfer characteristics measured at cryogenic temperatures are shown in fig. 2. The curves prove the independent electrical control of each electrode on the drain current.

A higher subthreshold slope was measured at 10 mK in a common-top gate configuration (i.e., with same voltage

applied to the barrier and front gates, fig. 2a). Higher currents were measured for decreasing temperature (fig. 2b and 2c) for similar overdrive voltages thanks to an enhancement of the electrons mobility [17]. A small mismatch in the barrier gates due to imperfect alignment of the electrodes is present, as shown in fig. 2b. For $|V_{DS}|$ voltages greater than 5 mV, no oscillations were measured whereas Coulomb blockade signatures were observed for selected V_{FG} voltages and -5 mV $\leq V_{DS} \leq 5$ mV, as evidenced by the non linearity in the plots in fig. 2b and 2d.

Room temperature measurements of the ultra-thin film devices for several back-gate bias configurations are shown in fig. 3. $I_{DS}(V_{FG})$ curves shift towards lower V_{FG} when the back-gate voltage is swept from negative to positive values until volume inversion (i.e., total inversion of the silicon film) is reached. The estimated back-gate threshold voltage is $V_{BGTH} \approx 1.45$ V and it has a dependence on V_{FG}, as shown in fig. 3b. Increasing off-currents were observed for decreasing V_{BG} and small negative values ($< |-1|$ nA) were measured for $0\,V < V_{BG} < V_{BGTH}$, as can be seen from fig. 3a and fig. 3d. This is related to the accumulation of holes and electrons at the interface between the BOX and the low doped handle wafer for positive and negative V_{BG}, respectively. This is confirmed by the poor V_{TH} control of the back-gate for $0\,V < V_{BG} < 0.8\,V$, where the substrate/BOX interface is brought from depletion to accumulation, as better illustrated in fig. 4a. In the ideal case of a metallic back-gate, the depletion capacitance does not take form and the following relation holds:

$$V_{TH} = V_{TH0} - \frac{t_{gox}}{t_{box}} \frac{1}{1 + \frac{t_{Si}}{t_{box}} \cdot \frac{\epsilon_{ox}}{\epsilon_{Si}}} V_{BG}, \qquad (1)$$

where V_{TH0} is the front-gate threshold voltage at $V_{BG} = 0$ V and t_{gox}, t_{box} and t_{Si} the gate oxide, buried oxide and top Si thicknesses. An almost linear $V_{TH}(V_{BG})$ relation was measured even with a low doped substrate with a maximum linear coefficient (body factor γ) given for strong accumulation at the substrate/BOX interface, where the electric field in the BOX is high enough to displace the top inversion layer from the top interface, increasing the back-gate capacitance.

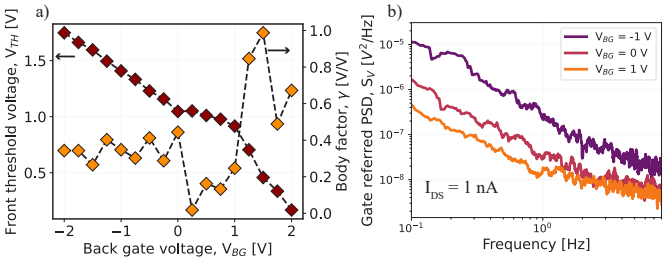

Fig. 4. a) Front gate threshold voltage dependence on back-gate voltage. The body factor is computed as the slope of the $V_{TH}(V_{BG})$ curve and it is maximized for positive V_{BG} biases. b) Frequency dependence of the gate referred power spectral density measured at room temperature. A lower $1/f$ noise is measured for a positive substrate bias.

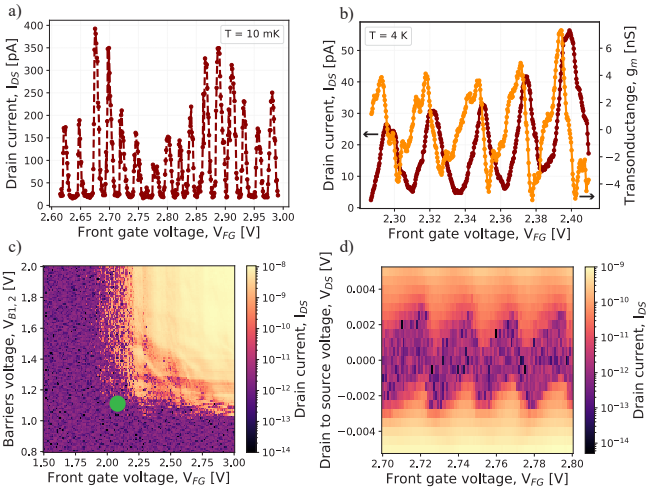

Fig. 5. a) Coulomb blockade oscillations measured at 10 mK with $V_{DS} = 1$ mV. b) Coulomb blockade oscillations measured at 4 K ($V_{DS} = 1$ mV), positive and negative values of the transistor transconductance are plotted as a function of the front gate voltage. c) Drain current measured at 10 mK for several barrier gates and front gate voltage combinations. The green dot indicates the conduction corner for which Coulomb oscillations are enabled. d) Periodic Coulomb blockade diamonds measured at 10 mK.

B. Impact of back-gate bias on drain current noise

The spectral components of the current noise in the ultra-thin film devices was analysed at room temperature for different V_{BG}. Specific front and back gate voltages were selected to give a constant drain current of 1 nA and currents were sampled for 4 min at 1 kSa/s. Three measurements for each configurations have been averaged to compensate for statistical noise from the setup. Results for the gate-referred power spectral density (PSD) are shown in fig. 4a, where

$$S_V = \left(\frac{1}{gm^2}\right) S_I, \qquad (2)$$

being S_I the drain current PSD and $gm = dI_{DS}/dV_{FG}$ (values extracted from the curves in fig.3a). The noise is reduced for $V_{BG} > 0$ V; this effect is commonly explained in terms of displacement of inversion carriers centroid from the top Si/SiO_2 interface [18]. At a fixed V_{FG}, this displacement is accompanied with an enhancement of the electrons mobility and higher currents are measured for increasing back-gate bias, as shown in the curves in fig. 3c with $V_{BG} << V_{BGTH}$.

C. SET characteristics

The SET operation was tested at 10 mK and 4 K. Coulomb oscillations are visible in the $I_{DS}(V_{FG})$ plots in fig. 5a and 5b. The periodicity of the drain current peaks is 25 mV and the extracted gate-to-dot capacitance is 6.4 aF. An equivalent dot radius of 36 nm was estimated according to a disk self-capacitance model. Broader peaks were measured at 4 K, where the thermal energy is not negligible compared to charging energy of the quantum dot. Positive and negative differential conductance values (g_m) of the transistor are plotted in fig. 5b.

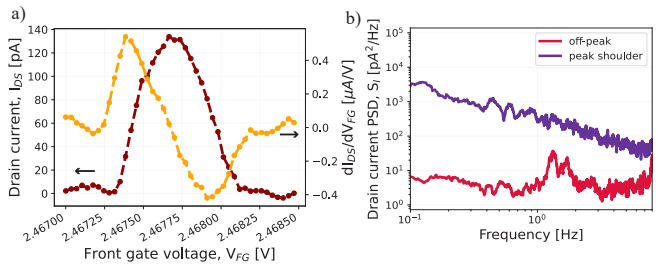

Fig. 6. a) Single current peak measured at 10 mK with $V_{DS} = 0.5$ mV and current sensitivity to front gate voltage. b) Power spectral density of the SET current measure at the points of maximum and minimum sensitivity; a peak at 1.4 Hz was measured, it is due to the pulse tube of the refrigerator.

For an accurate tuning of the device, drain current measurements were taken sweeping both front and barrier gates voltages. As shown in the color plot in fig. 5c, no conduction was enabled for barrier voltages below 1.1 V and front gate voltages lower than 2 V (at $V_{DS} = 1\,mV$).

We biased the device to work at the conduction corner (green dot in fig. 5c) to analyze Coulomb blockade dependence on V_{DS} and V_{FG} with fixed potential barriers. A slight difference of $10\,mV$ was set between the two barriers to compensate for the small asymmetry in the transfer characteristics. Regular Coulomb diamonds were measured for $V_{FG} >> V_{TH}$, as shown in fig. 5d. Here we report data for a selected window of V_{FG} values for which constant diamonds dimensions were measured. For lower bias voltages, dimensions changed as a function of front-gate and barriers voltage. For a better control on the dot chemical potential a more complex architecture including a single plunger gate and lateral inversion gates should be adopted.

Different source of noise can be studied analyzing the PSD of the drain current when the SET is biased at its maximum sensitivity point. An example of an SET noise measurement is shown in fig. 6. A single peak was selected and sampled for 5 min to ensure the stability of the device and instrumentation over time. Then, the device was biased at the points of maximum and minimum sensitivity and the drain current sampled for 5 min; results are shown in fig. 6b. Typical $1/f$ noise was measured at the maximum dI_{DS}/V_{FG} point, white noise was sampled elsewhere. The noise levels are comparable to the ones reported in [19].

IV. Conclusion

We have reported the fabrication and characterization of four-gated FD-SOI SETs on thin and ultra-thin film substrates. Measurements were taken at room and cryogenic temperatures proving the functionality of the devices when operated both as FETs and SETs. Back-gate characterization was performed at room temperature on ultra-thin film devices and the electrical noise has been analysed. Coulomb blockade oscillations were measured at 4 K and 10 mK in SET operation and current noise measurements have been reported to prove the stability and sensitivity of the SET when operated as a charge sensor. We have found that the regime of operation could influence both sensitivity and charge noise levels as the displacement of inversion carriers centroid from the Si/SiO_2 interface can be dynamically controlled. This experimental work is a step forwards towards the development of optimized multi-gate FD-SOI planar quantum dot based quantum devices with tunable properties by electrostatic control.

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