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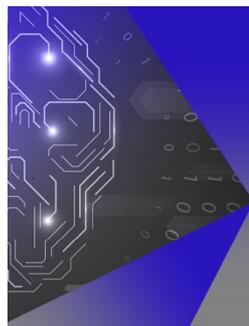
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ABSTRACT

We developed a process to fabricate nanoscale metallic gate electrodes on scanning probe cantilevers, including on the irregular surface of protruding cantilever tips. The process includes a floating-layer technique to coat the cantilevers in an electron-beam resist. We demonstrate gate definition through a lift-off process and through an etching process. The cantilevers maintain a high force sensitivity after undergoing the patterning process. Our method allows the patterning of nanoscale devices on fragile scanning probes, extending their functionality as sensors.

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INTRODUCTION

Cantilevers are widely used in scanning probe microscopy, where they find application as force transducers in, e.g., atomic force microscopy (AFM), magnetic force microscopy, and Kelvin probe microscopy.¹ These cantilevers are usually optimized for mechanical properties² and include only simple tip design features. The integration of more advanced sensors on cantilever tips would allow the combination of extremely sensitive detectors, such as superconducting quantum interference devices,³ single-electron transistors and quantum dot devices,^{4,5} and other quantum sensors with the navigational toolbox that scanning probe microscopy cantilevers provide. Such advanced devices typically require the patterning of multiple metallic or superconducting gate and contact electrodes of nanoscale dimensions.

Electron beam lithography (EBL) is a widespread technique to pattern nanoscale structures, such as gate electrodes. EBL can achieve a high patterning resolution, in practice resulting in smallest feature sizes of ~ 10 nm.⁶ Moreover, EBL enables batch production, and many standard recipes have been previously developed, facilitating a fast fabrication development process and high device yield. Typically, in EBL, a planar substrate is first spin-coated with a resist, which is subsequently irradiated with electrons, developed,

and processed further. However, spin-coating of small samples and substrates with non-flat surfaces does not provide a resist layer of acceptable uniformity due to effects such as edge-beading, lift-off problems, and an imperfect pattern transfer. Nonetheless, there are many applications where EBL on such irregular substrates would be of interest.

Various other techniques of coating such substrates with a resist layer exist, including spray coating,⁷ the use of ice resists,⁸ evaporative methods,⁹ and resist transfer techniques.^{10–12} Furthermore, focused-ion or electron-beam deposition¹³ and milling methods can be used to pattern irregular substrates. However, these techniques are either slow, are expensive, are only demonstrated for photoresists, or are not tailored toward patterning on fragile substrates, such as scanning probe microscopy cantilevers, which are vulnerable suspended structures with a length typically of the order of $100\ \mu\text{m}$ and a width and thickness of only a few μm .

Based on an approach used for patterning on flakes of 2D materials,¹⁴ we developed a fabrication process to pattern nanoscale structures on prefabricated cantilevers through EBL. The process involves coating the cantilever with an electron-beam resist using a floating-layer method. We fabricate metallic gates on various cantilever geometries, including on the sloped and tipped parts of the cantilevers. We demonstrate two methods of gate definition: a

lift-off process and an etching process. By employing either a standard electron-beam irradiation dose or a much higher dose, we use a poly(methyl methacrylate) (PMMA) layer either as a (standard) positive resist for the lift-off process or as a negative resist for the etching process. The process allows us to produce gate arrays with a gate width down to 70 nm and a pitch down to 90 nm. We have successfully applied the method to pattern different types of cantilevers with good reproducibility.

FLOATING PMMA METHOD

Figure 1 schematically shows the key steps of our floating-layer resist coating method. First, a 15% solution of dextran in deionized (DI) water is deposited onto a clean glass slide and spun at 2000 rpm for 40 s. Afterwards, the slide is baked at 150 °C for 3 min. The desired resist layer is then spin-coated on top of the dextran film. For the work shown here, we employ as resist 4.5% PMMA with 950 K molecular weight dissolved in anisole (Allresist AR-P 672.045). The PMMA is spun at 4000 rpm for 40 s and baked at 150 °C for 3 min, resulting in a resist layer thickness of ~230 nm [Fig. 1(a)]. Submerging the prepared slide into DI water for about 15 min causes the dextran film to dissolve [Fig. 1(b)]. After this, the slide is removed from the water, tilted by a small angle, and slowly inserted back into the water. This causes the PMMA to peel off the glass slide and float on the water surface, as illustrated in Fig. 1(c).

Next, the desired sample is fixed onto a metal holder. In our case, we use a non-contact atomic force microscopy cantilever (NanoAndMore ATEC-NC) and fix it to an aluminum square slide with Kapton tape [Fig. 1(d)]. We find that it is beneficial for the adhesion of the resist to the sample to perform UV-ozone plasma treatment for 5 min. To coat the sample with the floating PMMA layer, it is turned upside down [Fig. 1(e)] and slowly lowered into the floating PMMA until the sample is fully submerged, as shown in Fig. 1(f). The sample is then removed from the water at a small angle. To remove residual water, the sample is first dried with tissues, followed by a baking step at 150 °C for 3 min. This results in a sample that is coated by a uniform layer of PMMA [Fig. 1(g)], with minimal wrinkles or bubbles.

We use this method of resist transfer to demonstrate EBL patterning of gate electrodes using a lift-off process and using an etching process in the sections titled “GATES ON CANTILEVERS—LIFT-OFF PROCESS” and “GATES ON CANTILEVERS—ETCHING PROCESS”, respectively. The lift-off process is an additive technique, where a thin metallic layer is deposited on top of the patterned and developed a positive resist. In a next step, the resist is washed

away in a solvent, leaving the deposited material only in the areas where the resist was exposed. This technique is useful when etching or metallization can damage parts of the substrate material, for instance, when producing electrical contacts to semiconductor nanostructures or fragile 2D materials. The etching process is a subtractive technique, where a thin metallic layer is deposited onto the sample prior to deposition of the resist. The negative resist is then patterned and developed, after which the deposited layer is etched away only where the resist is not exposed. Such an etching process avoids problems associated with lift-off, such as retention of residual resist and the deposited material in unwanted areas of the substrate, and can produce finer structures than possible through lift-off.

GATES ON CANTILEVERS—LIFT-OFF PROCESS

In order to define gates using the lift-off process, we first structure the non-contact AFM cantilever using focused ion beam (FIB) milling. Originally, the slope of the AFM tip with respect to the main cantilever surface is 54.7°, resulting from the anisotropic KOH etching of silicon used to fabricate the cantilevers. We successfully cover the cantilevers with such large slope angles with PMMA and perform EBL, showing a good pattern transfer after development. However, with these large slope angles, we find that the lift-off process does not fully remove the unexposed parts of the resist in the tip area. To improve the lift-off, we, therefore, prestructure the tip by milling away part of it, adjusting its slope to ~30° [see the inset of Fig. 3(a)]. We also mill away selective parts of the tip in this step, resulting in a flat mesa at the top of the tip [see Fig. 2(a)], which is used as a platform to host a set of parallel gate electrodes. Note that structuring the cantilever tip area can be done already during cantilever fabrication, allowing to mass-produce cantilevers with the required tip geometry.

Before fabricating the gates, we use atomic layer deposition (ALD) to cover the cantilever with a 60 nm thick layer of Al₂O₃ [Fig. 2(b)], which later acts as an insulating layer between the metallic gates and the highly doped silicon cantilever body. Using the floating-layer method described before, we then coat cantilevers with PMMA [Fig. 2(c)]. Here, we coat the cantilevers with three layers of 950 K PMMA resist, each spun at 4000 rpm for 40 s and baked at 150 °C for 3 min, leading to a total resist thickness of roughly 690 nm. We align on characteristic points of the cantilevers to define the markers (Ti/Au, 5/50 nm) in a first standard EBL step. A second EBL step is employed to define the gate patterns [Fig. 2(d)], using the predefined markers. The resist is exposed using an acceleration

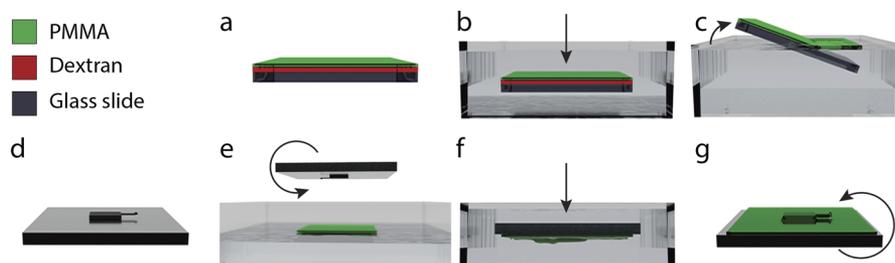


FIG. 1. Overview of the resist-coating process. The legends are shown in the top left. (a)–(c) Illustration of the preparation of a floating PMMA resist layer. (d)–(g) Illustration of the coating of a cantilever with the floating PMMA layer. See the main text for a detailed step-by-step description of the process.

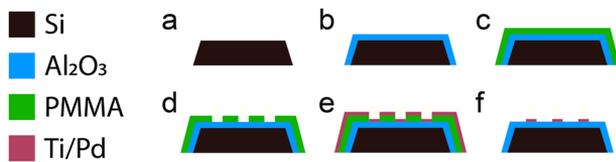


FIG. 2. Protocol of gate patterning through the lift-off process. (a) Side view of the prepatterned flat mesa on a cantilever tip. (b) The mesa is covered with a dielectric layer using ALD. (c) Floating PMMA transfer. (d) Definition of the gate pattern through EBL. (e) Electron beam evaporation of Ti/Pd. (f) The lift-off yields the desired nanostructures.

voltage of 30 kV and a dose of $375 \mu\text{C cm}^{-2}$, followed by development in isopropyl alcohol (IPA):methyl isobutyl ketone (MIBK) (3:1) for 60 s and IPA for 60 s. Afterward, 5 nm Ti and 25 nm Pd are deposited using an electron beam evaporator [Fig. 2(e)]. For lift-off, the sample is submerged in acetone for at least 1 h at 50°C [Fig. 2(f)].

Figure 3 shows scanning electron micrographs of cantilevers patterned with gates using our method. In Fig. 3(a), the tip is modified using FIB milling, as described. Three gates with a width of 350 nm and a pitch of 400 nm are fabricated on the cantilever, including on the sloped tip area. For Fig. 3(b), we use one layer of resist (230 nm) and pattern five nanoscale gates (width: 70 nm; pitch: 90 nm) on a flat cantilever. The nanoscale gates are patterned such that they connect to larger, prefabricated contacts that widen out to bond pads on the cantilever base.

GATES ON CANTILEVERS—ETCHING PROCESS

In order to be able to fabricate gates on cantilever tips with higher slopes, we developed an etching process that does not require a lift-off step, thus avoiding the problems due to incomplete material lift-off. By overdosing the same type of PMMA as before, it can be used as a negative resist¹⁵ and act as a mask for pattern transfer through subsequent etching. This process is, therefore, complementary to the one described before and more suitable for removing large parts of a metallic film.

Figure 4 schematically shows our top-down fabrication strategy to fabricate on a steep slope, as, for example, on the 54.7° slope of commercially available tipped cantilevers. As before, we start with such a cantilever where a mesa is cut using FIB [Fig. 4(a)], to host the nanoscale gates at the end of the cantilever tip. Next, 20 nm of Au is deposited using an electron-beam evaporator [Fig. 4(b)]. As shown in the work of Cai *et al.*,¹⁵ overdosing a conventionally positive PMMA resist allows us to use it as a negative resist. To coat our lever, we use the technique described in Fig. 1 [Fig. 4(c)]. Next, the PMMA layer is exposed to electron beam radiation at a high dose of $80\,000 \mu\text{C cm}^{-2}$ using an acceleration voltage of 30 kV. Afterwards, the sample is developed in acetone for 10 min and in IPA for 2 min [Fig. 4(d)]. Then, argon ion beam etching (60 s at 0° angle and 60 s at 40° angle, 500 V, 20 mA) is used to transfer the pattern of the negative PMMA resist to the Au film [Fig. 4(e)]. The last step of the process is to remove the overexposed PMMA, which is done by using oxygen reactive ion etching for 10 min at 120 W [Fig. 4(f)]. Figure 5 shows a scanning electron micrograph of a cantilever patterned using the

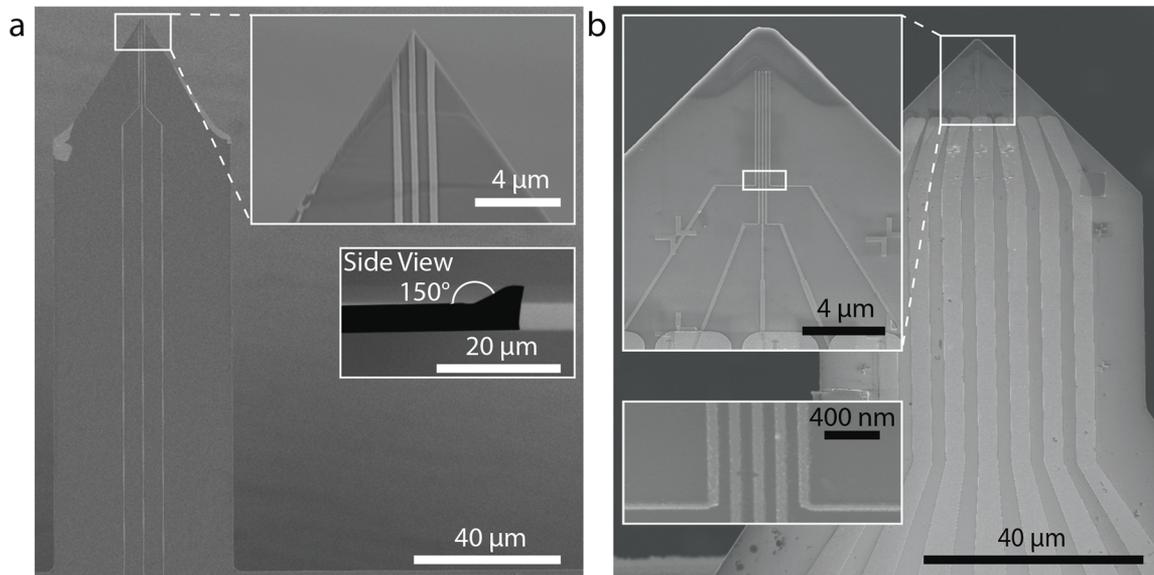


FIG. 3. Scanning electron micrographs of cantilevers with gates produced through the lift-off process. (a) Tipped cantilever with three Ti/Pd gates. Insets: zoom-in view of the tip area (top) and side view of the cantilever tip part (bottom). (b) A flat cantilever with seven large Au gates connected to five finer Ti/Pd gates in the front part of the cantilever. Insets: zoom-in images of the front of the cantilever, showing finer gates. Note that the marker structures seen here are deposited together with the finer gates and are used for subsequent lithography not discussed here. The bottom inset is a zoom-in image of the area delineated by a white box in the top inset. Note that focusing of the electron beam on specific cantilever parts for alignment purposes results in selective additional metallization, such as the rectangular piece on the right side of the cantilever in (b).

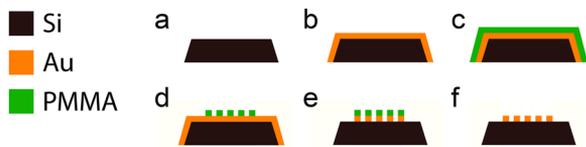


FIG. 4. Protocol of gate patterning through the etching process. (a) Side view of the prepatterned flat mesa on a cantilever tip. (b) Electron beam evaporation of Au. (c) Floating PMMA transfer. (d) The gates are patterned using overdosing of PMMA. (e) Argon ion beam etching transfers the pattern into the Au layer. (f) The resist is removed using oxygen reactive ion etching, yielding the desired nanostructures.

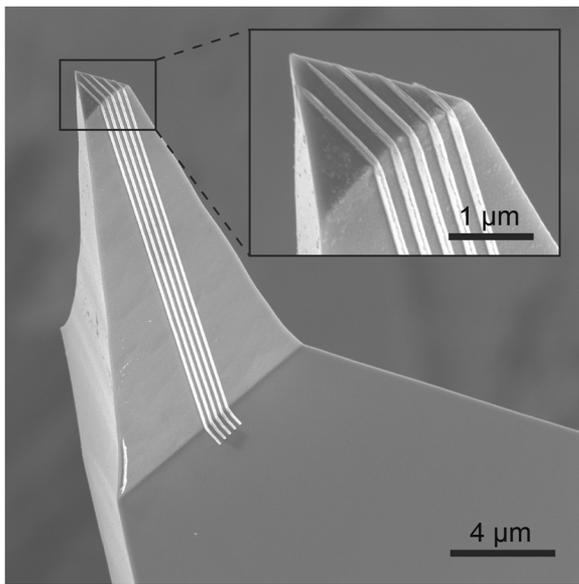


FIG. 5. Scanning electron micrograph of the tipped end of the cantilever, patterned with a gate array defined through the etching process.

described etching process. Five gates of 100 nm width and 180 nm pitch are fabricated on the tipped end of the cantilever featuring the original 54.7° slope.

MECHANICAL PROPERTIES

For the cantilevers to maintain their function as sensitive scanning probe force transducers, it is important that their mechanical properties remain unaffected by the lithography processes. To evaluate this, we measure (in high vacuum, at room temperature) the resonance frequency and quality factor of the first flexural mode of a cantilever, before and after processing. For the measurements, we use a piezoelectric actuator to drive the cantilever motion and an optical interferometer to detect the cantilever displacement. First, we find the resonance frequency of the cantilever's first flexural mode by sweeping the frequency of the piezoelectric drive while measuring the resulting cantilever displacement amplitude. Next, we measure the quality factor using a ringdown method, in which we first excite the cantilever resonance and, after stopping this excitation, measure

the exponential decay of the cantilever displacement amplitude as a function of time. The quality factor is then inferred from the time constant of this decay. Before processing, we measure a tipped cantilever with a quality factor of 80 k and a resonance frequency of 306.8 kHz. Next, we test the effect of our floating PMMA coating and lift-off process, first without any metal deposition. Here, we find no significant change in resonance frequency or quality factor. Finally, we measure after performing the lift-off process, this time with deposition of 5 nm Ti and 25 nm Pd gates, as shown in Fig. 3(a). Now, the resonance frequency is decreased to 301.4 kHz and the quality factor is decreased to 70 k. The decrease in the resonance frequency is expected due to the higher mass of the cantilever. The decrease in the quality factor results in a modest decrease in the thermal force sensitivity by <15%.

OUTLOOK

In future work, the resolution of the gate patterns could be improved by the use of thinner PMMA layers or by etching down the developed PMMA layer before pattern transfer.¹⁵ An interesting use of our method would be to pattern superconducting devices, such as superconducting quantum interference devices³ or charge qubits¹⁶ of small dimensions, on cantilever tips. This would enable sensitive imaging of nanoscale magnetic fields and charge dynamics with a high resolution, for instance, in 2D materials¹⁷ or qubit devices.¹⁸ Finally, although not tested here, our method could be used to perform EBL on various other types of samples with irregular surfaces, e.g., to pattern nanostructures on the facets of cleaved optical fibers.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

L. Forrer: Conceptualization (equal); Investigation (equal); Methodology (equal); Visualization (equal); Writing – original draft (lead); Writing – review & editing (equal). **A. Kamber:** Conceptualization (equal); Investigation (equal); Methodology (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **A. Knoll:** Methodology (supporting); Resources (equal); Writing – review & editing (equal). **M. Poggio:** Conceptualization (equal); Funding acquisition (equal); Investigation (supporting); Methodology (supporting); Project administration (equal); Resources (equal); Supervision (equal); Writing – original draft (supporting); Writing – review & editing (equal). **F. R. Braakman:**

Conceptualization (equal); Funding acquisition (equal); Investigation (equal); Methodology (supporting); Project administration (equal); Resources (equal); Supervision (equal); Writing – original draft (lead); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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