Nanomole Process: Enabling Localized Metallic Back-Gates for Enhanced Cryogenic Front-to-Back Coupling in FDSOI Quantum Dots

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***Abstract*—This paper introduces a novel integration method of localized metallic back-gates into fully-depleted silicon-on-insulator (FDSOI) multi-gate FETs, enabling robust front-to-back electrostatic coupling from room temperature to cryogenic conditions, without the need for substrate implantation. The fabrication process, termed the Nanomole process, utilizes nanometric vapor-phase etching of the buried oxide or silicon substrate with vapor-HF and XeF_2 gases. This is followed by atomic layer deposition (ALD) of a dielectric material and Pt, with precise patterning achieved through inductively coupled plasma etching. Detailed analysis of the process demonstrates controllable etching rates based on device geometry, providing calibrated guidelines for scalable manufacturing. Symmetric mid-*k* dual-gating is reported in devices featuring a Si-film thickness of 24 nm, with a top and bottom gate oxide equivalent thickness (EOT) of 6.5 nm. Electrical characterization of multi-gate FDSOI SETs, operated as FETs, confirms effective threshold voltage tuning through dual-gate operation, with consistent performance from room temperature to millikelvin regimes. Additionally, quantum mechanical simulations based on the effective mass approximation at 4 K offer insights into the electrostatic behavior of dual-gated SOI quantum dot devices in both planar and nanowire geometries. This scalable and versatile technological solution opens new possibilities for advanced quantum devices, such as charge and spin qubits, by enabling in situ control over volume inversion, electron valley splitting, and spin-orbit interaction.**

***Index Terms*—Cryo-CMOS, FDSOI, quantum dots, vapor phase etching, back-gate, dual-gate control, volume inversion, valley splitting, nanomole process.**

I. Introduction

Silicon-based quantum technologies, including electron and hole spin qubit devices, have advanced significantly in recent years, driven by improvements in fabrication techniques and material optimization [1]. These advancements have been demonstrated in 2D and 1D qubit arrays in planar structures, such as ^{28}Si/SiGe heterostructures [2] and planar Ge [3], as well as in Si metal-oxide-semiconductor (MOS) architectures inspired by nano-CMOS technology, including bulk silicon FinFETs [4] and fully-depleted silicon-on-insulator (FDSOI) nanowires [5]. This further motivates technological efforts towards a large-scale co-integration of classical and quantum processing units [6], essential for efficiently controlling sparse arrays of single- and two-qubit gates [7].

FDSOI substrates are widely used in analog and digital applications due to their excellent device isolation, ultra-low power consumption, and dynamic threshold voltage tuning via back-gate biasing. These advantages extend from room temperature to cryogenic conditions [8], [9], [10], making FDSOI promising for cryoelectronics and quantum computing [11], [12], [13], [14], [15]. This potential is further highlighted by recent advancements in compact 22nm FDSOI CMOS designs, including inductorless transimpedance amplifiers [16] and multiplexers [17] for spin qubit array readout, as well as monolithic control units for fluxonium qubits [18]. Additionally, efforts are underway to integrate ferromagnetic layers for electric dipole spin resonance (EDSR) at the front-end-of-line (FEOL) level [19], [20], leveraging the substrate isolation provided by the buried oxide (BOX).

In FDSOI spin qubits, dual-gate control can induce a high transverse electric field across the heterostructure, modulating valley mixing and spin-orbit coupling while enabling all-electrical spin qubit manipulation [21]. Moreover, a back-gate can play a crucial role in mitigating charge noise (the primary source of decoherence in silicon spin qubits) which mainly originates from interface defects and coupling to reservoirs [22]. By electrostatically tuning the extension and position of quantum dots, the back-gate helps suppress these detrimental effects [23]. Several technological solutions have been adopted.

In their characterization studies, Roche et al. [24] and Spence et al. [23] enabled back-gate biasing through the silicon substrate via photoexcitation from an LED. While effective for static operation at high back-side voltages ($\approx$ 5-30 V), this approach is slow and does not allow local tuning of the semiconductor potential. Individual control of FDSOI devices below 4 K can be achieved by integrating reversely biased p- and n-wells or localized metallic contacts beneath the BOX. Fabrication techniques for this include frontside dopants im-

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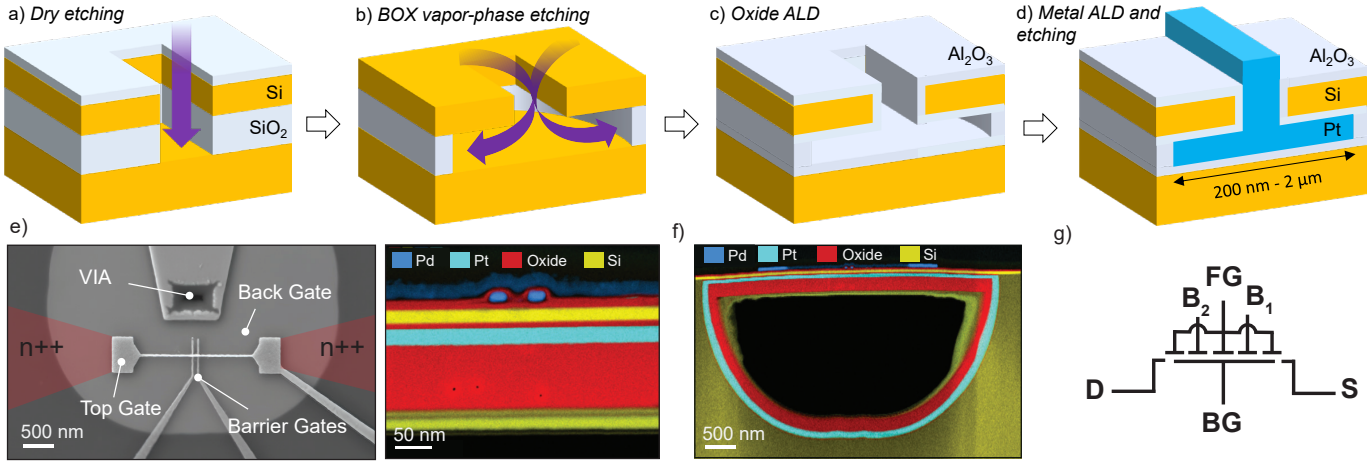

Fig. 1. Simplified description of the nanomole-BOX process for integrating a localized metallic back-gate in SOI substrates. a) ICP dry etching for via patterning, b) vapor phase HF etching of the SiO_2 BOX, c) ALD of an oxide layer (Al_2O_3 shown as an example), and d) ALD metallization and contact patterning. e) SEM image of a fabricated multi-gate SET with metallic back-gate, along with TEM-EDX material analysis of the device cross-section taken at the top-gate position. The equivalent oxide thickness (EOT) of both top- and bottom-gate oxides is 6.5 nm (15 nm of Al_2O_3), while the silicon thickness is 24 nm. f) Cross section of a device with TEM-EDX analysis showing the maximum achievable etching depth enabled by the nanomole process. g) Circuit schematic of the device.

plantation [25] and methods for accessing the bottom interface of the BOX, such as Bosch dry etching, KOH wet etching, or advanced SOI substrate engineering [26].

In the microelectronics industry, double-gate FDSOI MOSFETs are commonly fabricated using dopant implantation [27]. However, ion implantation through the SOI channel and BOX layer requires high-energy beams, which can amorphize the channel region and introduce unintended dopant densities in the active area of the device. This presents challenges for FDSOI quantum dots and spin qubits, as their performance is highly sensitive to crystalline and interface defects, as well as hyperfine interactions with dopant atoms. The problem is further compounded by the widespread use of isotopically purified ^{28}Si, specifically engineered to improve qubit coherence times. While implementing a metallic contact through back-side etching may be effective for laboratory investigations [28], this approach lacks scalability and alignment precision due to the typical thickness of large silicon substrates (generally exceeding 225 μm). These limitations hinder its viability for large-scale integration. A promising alternative is the use of a localized metallic back-gate patterned via front-side lithography, with its fabrication enabled by the so-called *nanomole* process [29].

II. Metallic Back-Gate in SOI

The key advantage of the *nanomole* process over conventional back-side etching methods is its precise localization of the back-gate, achieved through frontside lithographic alignment on commercial SOI substrates. CMOS-compatible vapor-phase etching with hydrofluoric acid (vHF) and XeF_2 enables selective bulk micromachining of SiO_2 and Si, respectively [30], [31], [32]. These processes facilitate controlled back-gate patterning by selectively etching either the BOX (*nanomole-BOX* process) or the underlying substrate (*nanomole-Si* process). Tunable etch rates, adjusted via gas pressure, allow for fine control over the back-gate dimensions. A detailed description of the process follows.

A. The Nanomole-BOX Process

Simplified schematics illustrating the key steps of the back-gate nanofabrication process for BOX etching are presented in Fig. 1, along with a scanning electron microscopy (SEM) image of a fabricated multi-gate single-electron transistor (SET) and energy-dispersive X-ray analysis (EDX) performed via transmission electron microscopy (TEM).

In the *nanomole* process, an electrical via is anisotropically etched next to the transistor channel through the SOI heterostructure using inductively coupled plasma (ICP) etching with SF_6/C_4F_8. The etching time is precisely controlled to stop at the top interface of the BOX, creating a window for isotropic etching of the buried SiO_2 with vapor-phase HF (vHF), using the SOI layer as a mask. In our process, the vHF etch rate was set to 18 nm/min by adjusting the gas pressure to 125 Torr. We note that the SiO_2 removal rate is influenced by the total exposed oxide in the chamber due to macro-loading effects, requiring vHF pressure calibration based on the sample size.

To protect the top gate oxide of the MOS gate stack (typically thermal-SiO_2), a capping layer of Al_2O_3 is used due to its significantly slower vHF etch rate ($\approx$ Å/min) compared to the buffered-HF etch rate ($\approx$ 70 nm/min). Holes ranging from 2 μm to 200 nm in radius were fabricated by adjusting the processing time, with the maximum achievable aspect ratio shown in Fig. 1f. The upper limit was determined by the largest hole size at which the suspended SOI membranes remained intact during etching and ALD steps.

Next, the etched hole is filled with a dielectric layer of arbitrary thickness (5–30 nm), followed by 10 nm of platinum (deposited using CpMePtMe precursor at 75 °C and O_2) via successive ALDs at 280 °C. This step enables the replacement of the BOX with mid-k or high-k dielectrics such as Al_2O_3 and HfO_2 for bottom-gating. Alternatively, the BOX can be

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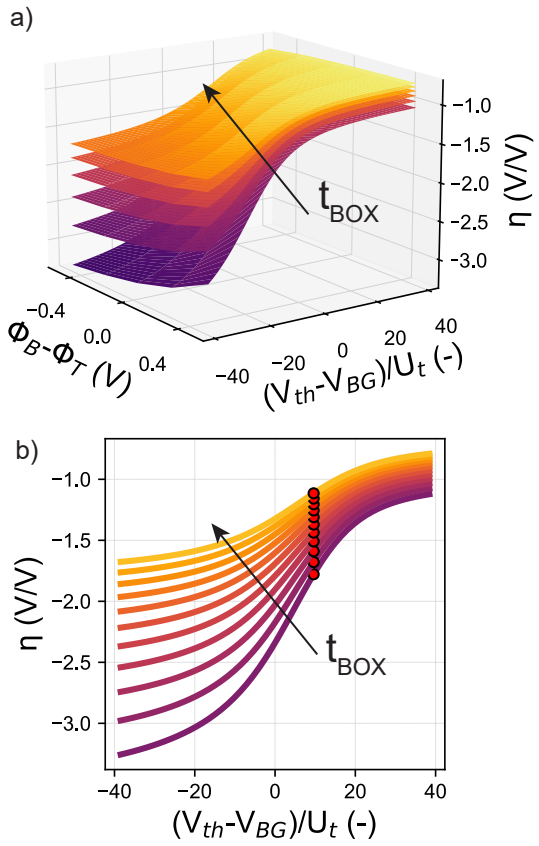

Fig. 2. FDSOI back-gate coefficient ($\eta = dV_{th}/dV_{BG}$) computed using Eq. 1. a) Dependence on the front-back workfunction difference, back-gate voltage, and oxide thickness plotted for the case of ALD-Al_2O_3 ($k \approx 9$) and SiO_2 (10 nm, $k \approx 3.9$) as bottom and top dielectrics, respectively. The thickness of the Si channel is 18 nm, the lowest curve is for $t_{box} = 10$ nm and the increment between the curves is $\Delta t_{box} = 2$ nm. b) Cut-plane of the 3D plot in (a) for $\phi_B = \phi_T$ showing η for oxide thicknesses ranging from 10 nm to 20 nm, with $\Delta t_{box} = 1$ nm. U_t is the thermal voltage, and the red dots highlight the discontinuity points in Eq. 2.

regrown through SOI thermal oxidation, controlled by oxygen diffusion through the via. The hole is then either completely filled with a dielectric or left open, similar to the silicon-on-nothing process [33]. If the hole size significantly exceeds the lateral dimension of the via ($l \approx 200$ nm), back-gates larger than the via remain unfilled, as the deposited layers primarily fill the via itself.

Finally, Pt is removed from the wafer surface by ICP etching using Cl_2/Ar, with different capping layers employed depending on whether back-gate integration was performed before or after front-gate fabrication (see Appendix A for details). Given that various dielectrics and metals [34], [35] can be deposited with ALD processes, the *nanomole* process provides a versatile platform for designing dual-gate FET control.

B. Engineering parameter space

The *nanomole* process provides several degrees of freedom for engineering of the dual-gate coupling. These include the bottom oxide thickness (t_{box}), the dielectric constant (k), and the work function difference between the bottom and top gates ($\Delta\phi = \phi_B - \phi_T$). We report the dependence of the back-gate coefficient $\eta = dV_{th}/dV_{BG}$ on these parameters, where V_{th} is the threshold voltage of the transistor in top gate operation, and V_{BG} is the back-gate voltage. The analysis is based on an analytical model for the FDSOI threshold voltage previously validated from room to cryogenic temperatures for both forward-back-bias (FBB) and reverse-back-bias (RBB) configurations [36]. This model determines η from the relation between the back and top gate transconductance of FDSOI transistors, assuming the drain current in subthreshold regime for the derivation. An analytical expression of η highlighting the dependence on the bottom-oxide capacitance C_{box}, the front-oxide capacitance C_{fox}, and channel capacitance C_{ch} is given in Eq. 1, with asymptotes listed in Eq. 2:

$$\eta = \frac{dV_{th}}{dV_b} = \frac{C_{box}}{C_{fox}} \frac{(C_{fox}(\theta - e^{\theta} + 1) - C_{ch}(\theta e^{\theta} - \theta))}{(C_{box}(\theta e^{\theta} - e^{\theta} + 1) + C_{ch}(\theta e^{\theta} - \theta))}, \tag{1}$$

$$\eta = \begin{cases} -\dfrac{1}{C_{fox}} \dfrac{C_{box}C_{ch}}{C_{box}+C_{ch}} & \text{if } V_{bg} \to -\infty \\ -\dfrac{C_{box}}{C_{fox}} \dfrac{(2C_{ch}+C_{fox})}{(2C_{ch}+C_{box})} & \text{if } V_{bg} \to V_{th} - \Phi_{bf} \\ -C_{box}\left(\dfrac{1}{C_{fox}} + \dfrac{1}{C_{ch}}\right) & \text{if } V_{bg} \to +\infty \end{cases} \tag{2}$$

The parameter θ (defined in Eq. 3) represents the difference of semiconductor surface potential (ψ_s) between the top (ψ_{st}) and bottom (ψ_{sb}) interfaces normalized by the thermal voltage U_t. Φ_{bt} is the workfunction difference between top and bottom gate metals, and the dependence of θ on the capacitances is described by $\alpha(C_{box}, C_{fox}, C_{ch})$, in Eq. 4:

$$\theta(V_{bg}, \Phi_{bf}, C_{box}) = \frac{\psi_{st} - \psi_{sb}}{U_t} = \frac{\alpha(V_{th} - V_{bg}) + \alpha\Phi_{bt}}{U_t} \tag{3}$$

$$\alpha = \frac{C_{box}C_{fox}}{C_{box}(C_{fox} + C_{ch}) + C_{fox}C_{ch}.} \tag{4}$$

The dependence of η on $C_{box}(t_{box})$, $\Delta\phi$, and back-gate voltage V_{bg} is shown in Fig. 2 for the case of ALD-Al_2O_3 (assuming $k = 9$). The model predicts high threshold voltage tunability with enhanced electrostatic control of the charge transport in the thin SOI film, showcasing unique dual-gate control enabled by the process.

C. Nanomole-Si Process: A BOX-Preserving Alternative

When patterning a back-gate beneath etched structures such as FDSOI FinFETs or nanowires, it is advantageous to retain the buried oxide while micromachining the silicon substrate. An alternative to the *nanomole-BOX* process involves injecting XeF_2 to etch holes in the Si substrate beneath the BOX, preserving the buried SiO_2 layer and maintaining a high-quality silicon-dielectric interface. A schematic of this method, referred to as the *nanomole-Si* process, is shown in Fig. 3(a–d).

In our fabrication, samples were exposed to two XeF_2 etching cycles (11 s each) at a gas pressure of 1 Torr. In this

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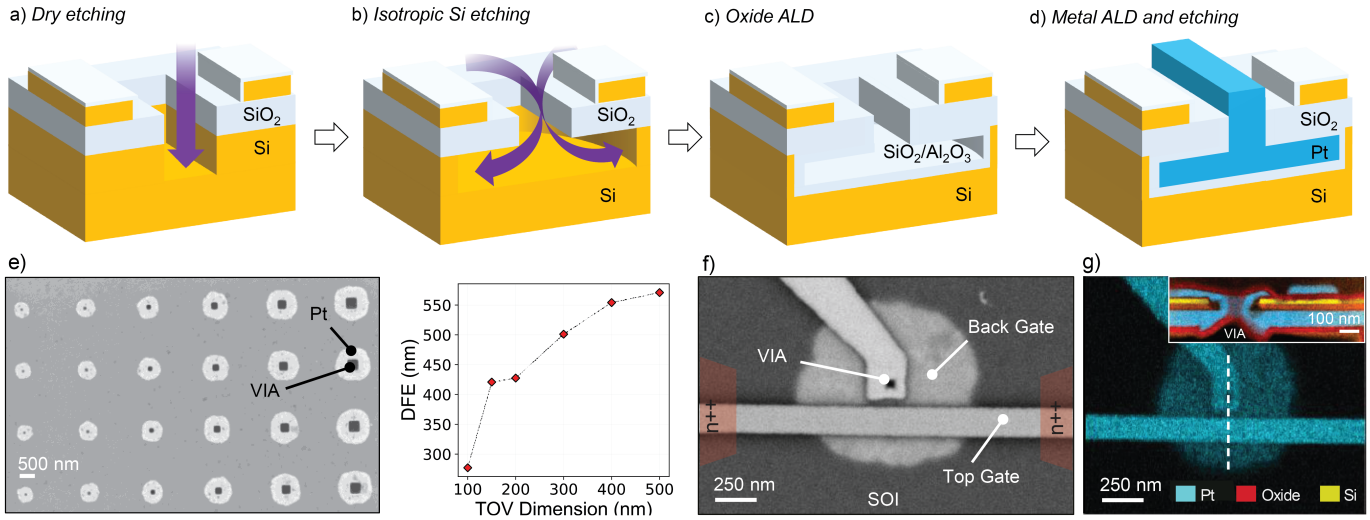

Fig. 3. Description of the nanomole-Si process. a) ICP dry etching for via patterning, b) isotropic etching of the silicon substrate using XeF_2 gas, c) ALD deposition of a thin oxide for back-gate insulation from the substrate, and d) ALD metallization and contact patterning. e) SEM image of fabricated back-gates beneath the BOX, showing the dependence of the maximum distance from the via edge (DFE) on the lateral dimension of the through-oxide via. f,g) SEM image of a fabricated FDSOI FET with SEM-EDX and TEM-EDX analysis of the materials. The inset in (g) shows a cross-section along the dotted line. The Si thickness is 18 nm, while the top oxide consists of 10 nm of Al_2O_3, and the BOX (SiO_2) is 20 nm thick.

step, the etched hole radius is strongly influenced by the lateral size of the via due to diffusion-limited reactant and product exchange, as reported in Fig. 3e. Further studies are needed to explore different combinations of XeF_2 pressure and via depths with varying SOI/BOX thicknesses.

Fig. 3(f–g) presents a successful metallic back-gate integration in a long channel FDSOI field-effect transistor (FET), along with SEM-EDX and TEM-EDX analyses of the materials. The electrical characterization of this proof-of-concept device is provided in Appendix A, Fig. 8.

III. Electrical Characterization of Front-to-Back Coupling

The electrical characterization of dual-gate coupling in an FDSOI SET (with same geometry and dimensions of the device in Fig. 1) operated as a MOSFET and fabricated with the nanomole-BOX process is reported in Fig. 4(a-d), with schematic of the top-gate configuration in Fig. 4e. The top-gate trans-characteristics dependence on FBBs applied to the back-gate are compared at room and cryogenic temperatures. The device was fabricated by replacing the BOX with 15 nm of Al_2O_3 for a symmetric dual-gate coupling, featuring a back-gate that spans the entire transistor channel and connects the source and drain implantated regions. Due to the higher dielectric constant of Al_2O_3 ($k \approx 9$) compared to SiO_2 ($k \approx 3.9$), a high back-gate coefficient η is expected. This is illustrated in Fig. 4d, which shows the dependence of V_{th} on V_{BG} from 300 K to 12 mK. The estimated threshold voltage is extracted by linear interpolation of I_{DS}/V_{TG} curves at the point of maximum transconductance [37]. The data show an almost linear voltage shift, with a slope that remains nearly independent of temperature. The experimental slope (dV_{th}/dV_{BG}) closely matches the analytical expression for an ideal metallic back-gate in FBB, which coincides with the $V_{BG} \to -\infty$ asymptote in Eq. 2:

$$V_{th} = V_{th0} - \frac{t_{gox}}{t_{box}} \frac{1}{1 + \frac{t_{Si}}{t_{box}} \cdot \frac{\epsilon_{ox}}{\epsilon_{Si}}} V_{BG}, \tag{5}$$

where V_{th0} represents the front-gate threshold voltage at V_{BG} = 0 V, and t_{gox}, t_{box}, and t_{Si} denote the thicknesses of the gate oxide, buried oxide, and top silicon extracted from TEM measurements, respectively. We attribute the net jump in threshold voltage between the 70 K and 1 K curves to the freezing of charge traps in the gate stack [38], which could be mitigated by incorporating annealing steps in forming gas during fabrication. Our characterization study indicates that the nanomole-BOX process is preferable to the nanomole-Si for achieving better electrostatic control. This is attributed to the ability to use higher-k dielectrics for bottom-gating and the lower surface roughness compared to silicon etching with XeF_2 [39]. Additionally, in the case of the nanomole-BOX process, employing a smaller via window has a minor effect on diffusion dynamics and back-gate dimensions, enabling the engineering of more compact device architectures.

IV. Dual-Gate Quantum Dots in SOI

The proposed localized back-gate can be integrated into both planar and MESA-etched (*i.e.*, 1D confined) SOI structures. We conducted quantum mechanical simulations at 4 K to analyze the electrostatic coupling between the top and back-gates in both configurations, to demonstrate dual-gate control of quantum dots with accurate charge displacement across the SOI film. The simulations assume the silicon Fermi level (E_F) lies within the band gap and locally lower the conduction band by biasing the control gate while keeping two barrier voltages fixed. Self-consistent calculations are performed using an in-house Schrödinger-Poisson solver [40] based on the effective mass approximation. The system is modeled

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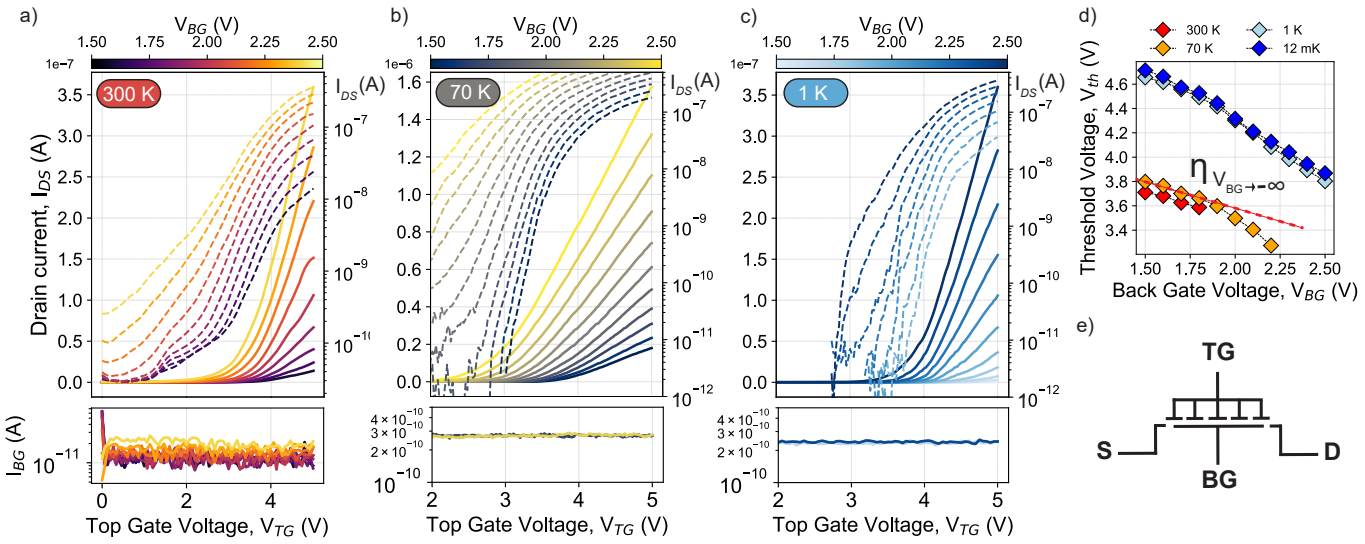

Fig. 4. Electrical characterization of the multi-gate SET, operated as a FET. The BOX layer is replaced with 15 nm of ALD-Al_2O_3 through the nanomole-BOX process. The top gate oxide is 15 nm of Al_2O_3, and the Si thickness is 24 nm, as in Fig. 1e. The estimated top gate length and width are 2.5 μm and 35 nm, respectively. a–c) Transfer characteristics and back-gate leakage (I_{BG}) measurements at 300 K, 70 K, and 1 K, respectively. The drain-to-source voltage (V_{DS}) is 500 mV. d) Threshold voltage dependence on back-gate bias from room temperature to 12 mK, with a linear fit (in red) computed from Eq. 2. e) Circuit schematic of the multi-gate FET, showing a back-gate extending beneath the channel.

with closed boundary conditions to prevent carrier injection from the contacts. The number of electrons in the quantum dot is determined by counting eigenstates with energy below E_F. The simulation runs until the first energy level crosses E_F, representing the doubly degenerate ground state of the quantum dot. It is worth noting that to map the charge stability diagram based on carrier injection through the barriers, this proof-of-concept study should be extended to self-consistent simulations with open boundary conditions. Nonetheless, in-depth investigation is required to include the relevant physics of electron spin system (*e.g.* magnetic respond, driving, valley-mixing). We restrict our initial analysis to electrostatic effects.

A. SET Electrostatics in Planar FDSOI Films

A 3D plot of the ground state isodensity surface defining a single-electron quantum dot within an FDSOI SET is provided in Fig. 5. By applying a slightly negative voltage to two barrier gates (V_B = -0.1 V), a localized density of charge is formed a few nm from the SOI interfaces through the symmetric contributions of a common plunger (top) and bottom gates (V_{CP} = 1.4 V, V_{BG}= 1 V). It is known that charge noise decreases as the quantum dot is less confined against an interface, where a large density of interface traps (D_{it}) is present. For a Si/SiO_2 interface, D_{it} is typically in the order of 10^{11} $cm^{-2}eV^{-1}$, and the density of charge traps can increase by several orders of magnitude for ALD oxides. Our simulations of cryogenic device operation demonstrate that charge confinement occurs at the core of the SOI film through calibrated front-back coupling, enabling control over volume inversion and mitigating charge scattering caused by interface imperfections.

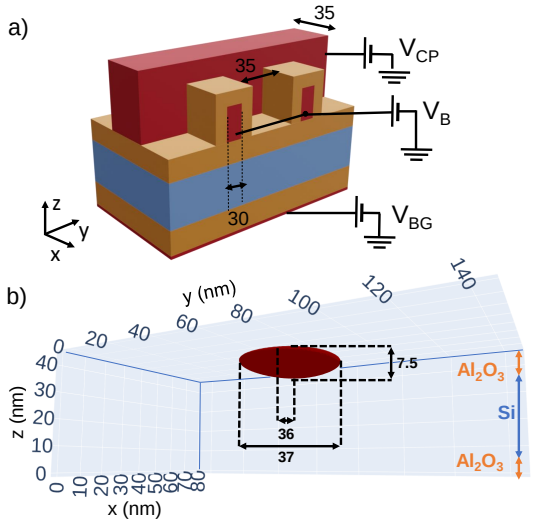

Fig. 5. Simulation results for an FDSOI SET featuring a common plunger gate, two barrier gates, and a back-gate. The metallic gates are illustrated in red, silicon in blue, and dielectric in orange. All dimensions are in given in nm. a) Schematic of the architecture with voltage biases applied to the four gates. b) Ground state isodensity surface within which 90 % of the total single electron charge is encapsulated. The dimensions of the isosurfaces along $\hat{x}$, $\hat{y}$, and $\hat{z}$ are indicated as double arrows.

B. Quantum Dot Control in FDSOI Nanowires

The geometry of a multi-gate FDSOI nanowire is given in Fig. 6a, along with the electrical gates used to tune quantum dot formation in Fig. 6b. A quantum dot is electrostatically confined through a combination of front-back coupling (V_P and V_{BG}) and depletion regions (induced by V_{BL} and V_{BR}). Simulations indicate that a quantum dot is formed at the upper interface between Si and Al_2O_3 when the following biases are applied: V_P = 1.6 V, V_{BG} = 0.6 V, and V_{BL} = V_{BR} = 1.4 V. As a preliminary result, we examine the spatial response of

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the single dot to a small bias modulation of the plunger gate or the back-gate. The bias is ramped in three steps: from 1.6 V to 1.55 V for the plunger gate, and from 0.6 V to 0.55 V for the back-gate. Fig. 7 shows the computed charge density as the squared wavefunction of one of the two degenerate states, the electrostatic potential, and the dimensions of the dot. The estimated quantum dot dimensions $l_{x,y,z}$ are obtained from:

$$s_w(r) = \sqrt{\frac{\sum_{n=1}^{n} w_i(r_i - \bar{r_w})^2}{\frac{M-1}{M}\sum_{n=1}^{n} w_i}} = \frac{l_r}{2}, \tag{6}$$

where s_w represents the weighted standard deviation, $\bar{r}$ is the weighted average position of the quantum dot along the direction r (with $r = x, y, z$), and n is the total number of discretization points i in this direction. w_i is the weight (charge density) at position r_i and M the number of non-zero weights. The simulations show that the gate modulation has minimal impact on the dot extent along $\hat{z}$, with L_z remaining approximately 3.6 nm for all bias configurations. However, in the xy-plane, the dot exhibits a more pronounced elliptical shape when the plunger-gate is modulated ($L_x > L_y$). Indeed, the dot anisotropy in this plane is inherited from a rectangular geometry of the contact gate area which primarily acts at the immediate dot location. In contrast, due to its larger coverage area, back-gate modulation has a homogeneous influence on the overall electrostatic potential found inside the channel, and thus leads to a more circular dot shape. These results underscore the importance of adequate front-back coupling for efficient control over the quantum dot profile.

C. Applications of Dual-Gate Control in Spin Qubits

Shaping and positioning quantum dots through the use of local back-gating holds interesting prospects for better control of spin qubits in Si-based devices. Such a method could for instance be used to directly control and increase the lowest valley splitting of electron spin qubits in Si [41]. This valley splitting is known from many experiments to be relatively small (typically ranging between 10s and 100s of μeV for e.g. Si/SiGe or Si/SiO_2 platforms), and close to the thermal energy and the Zeeman energy of the qubits (at operating temperatures and field of 0.1 – 1 K, and B = 0.1 – 1 T) [41]. Especially at lower energies, this can lead to thermal excitation of the valley degree of freedom, as well as spin-valley mixing, resulting in leakage out of the qubit computational subspace and increased decoherence and relaxation rates. This problem is exacerbated when operating at elevated temperatures of 1 K and above, which is viewed as an attractive operation regime for scaled-up quantum processors [42]. Moreover, the valley splitting is strongly sample- and even location-dependent, for instance due to fabrication process nonuniformities and interface disorder. The ability to tune the valley splitting in situ, and locally for individual quantum dot sites, would therefore allow minimizing such decoherence and relaxation channels. Various quantities can be used to control and increase valley splitting, including electric and magnetic fields, and strain [43]. In particular, electric fields can shape and reposition a quantum dot, which in turn can be used to steer the electron wave function into a position of increased valley splitting. Valley

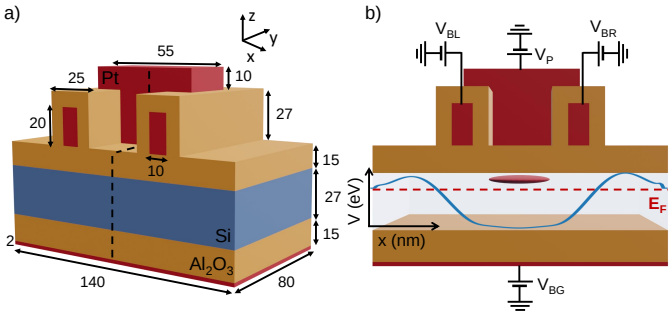
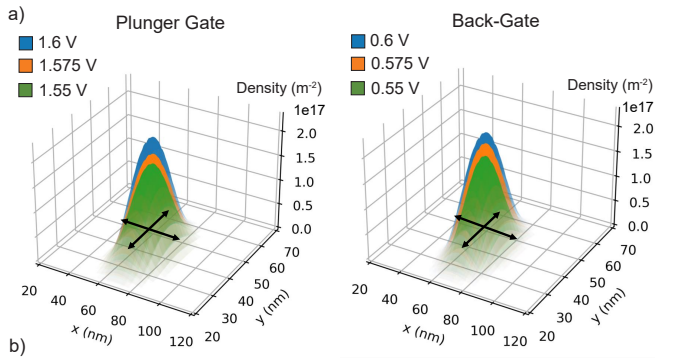


Fig. 6. Schematic of a multi-gate FDSOI nanowire. a) Illustration of the simulated device with dimensions in nm, all metallic gates are highlighted in red. b) Side view of the device showing the electrostatically-induced quantum dot (red ellipse). The blue curve represents the average electrostatic potential (Si conduction band) across the transistor channel (in transparency) and is controlled by four metallic gates: the plunger gate V_P, the back-gate V_{BG}, and the barrier gates V_{BL} and V_{BR}.

splitting may be controlled in this way by pushing the wave function to have larger overlap with material interfaces, or by moving it away from interface steps [44]. For Si fin-like structures, valley splitting may also be electrically controlled by pushing the wave function into regions of increased strain [45]. For hole spin qubits, the electric fields between top and back gates may be used as a knob for tuning system into sweet-spot operating regime, where spin-orbit interaction is large but decoherence due to charge noise is minimized [46], [47]. Such electrical tuning could then be used to tune effective g-factors and maximize Rabi frequencies [48], [49], whilst at the same time minimizing decoherence. Finally, the nanomole process potentially allows for producing back layers consisting of split gates with nanoscale dimensions. This would enable bringing in quantum dot control-lines not only from the topside but also the backside of the sample, alleviating problems with high-density routing of gates [50]. We note that the addition of a metallic back gate may lead to degradation of radio-frequency reflectometry read-out methods [51] of spin qubits. Here, the capability of defining small local back-gates may be an asset: one can pattern a back-gate only underneath the quantum dots hosting the qubits, while keeping the area underneath a nearby charge sensor without back-gate. Nevertheless, care will have to be taken to take into account the additional parasitic capacitance resulting from the nearby back-gate, for instance by incorporating a varactor in the read-out circuit [52].

V. Conclusion

We reported the fabrication and characterization of multi-gate FDSOI FETs with a localized metal back-gate designed for the cryogenic control of Si quantum dots and qubits. We developed the nanomole process, in which a scalable metallic contact with a radius ranging from 200 nm to 2 μm is selectively patterned beneath the transistor channel. This is achieved through nanometric vapor-phase etching of either the BOX or substrate, followed by filling with ALD dielectric and Pt. The functionality of dual-gate control has been experimentally validated from room temperature down



c)

V_{PG}	L_x	L_y	L_z
1.6 V	14.98	15.76	3.62
1.575 V	15.82	15.32	3.62
1.55 V	15.86	14.44	3.64

V_{BG}	L_x	L_y	L_z
0.6 V	14.98	15.79	3.62
0.575 V	14.84	14.80	3.58
0.55 V	13.48	13.22	3.52

(Dimensions of the quantum dot in nm)

Fig. 7. Simulation results for a multi-gate FDSOI nanowire. a) Charge density in the SOI controlled by the plunger and back gates, computed as the squared wavefunction of one of the first degenerate states with energy below E_F. Values are averaged over the film thickness (z). b) Electrostatic potential within the SOI nanowire, averaged in the y-z plane. The color legend follows the one in (a). c) Evolution of the quantum dot dimensions as a function of the plunger gate voltage (V_{PG}) and back-gate voltage (V_{BG}).

to millikelvin, demonstrating higher electrostatic coupling when replacing the SiO_2-BOX with mid-k dielectric (Al_2O_3). Quantum mechanical simulations based on the effective mass approximation at 4 K showed effective tuning of the quantum dot extension in the SOI film through back-gate biasing. This versatile technological solution for localized back-gate integration opens up new possibilities for tunable FDSOI qubits, potentially enabling control over volume inversion, spin-valley mixing, and spin-orbit coupling in Si quantum dots.

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Appendix A

Post- and Pre-Integration of Back-Gates:

We explored integrating the back-gate both before and after fabricating the front-gates. Due to the high energy required to etch the ALD-Pt from the top surface, a thick capping layer (25 nm) was initially deposited to protect the active area (*i.e.*, the transistor channel) of the device in both cases. When the back-gate was patterned as the final fabrication step, an ALD-SiO_2 capping layer was used, whereas an ALD-Al_2O_3 layer was employed when patterning it prior to the front-gates. This selection is based on the high etch selectivity of alumina over silicon oxide when treated with H_3PO_4 heated at 60 °C, that enables a safe removal of the protection layer before processing the front-gates.

Dual-Gate Control Enabled by the Nanomole-Si Process: The nanomole-Si dual-gate FET shown in Fig. 3f features a back-gate approximately 300 nm in diameter, positioned at the center of a long SOI channel electrostatically defined by the top-gate. The Pt back-gate only partially overlaps with the transistor channel. The electrical characteristics of the device measured at 300 K and 4 K are shown in Fig. 8(a-b), with the threshold voltage dependence and a schematic of the device in Fig. 8(c-d). Unlike the nanomole-BOX characteristics, the nanomole-Si device exhibits a significant change in the slope $\eta = dV_{th}/dV_{BG}$ between 300 K and 4 K, with reduced linearity compared to Fig. 4d. A full comparison between the nanomole-BOX and nanomole-Si approaches requires fabricating devices of varying dimensions on different substrates, this is left for future work.

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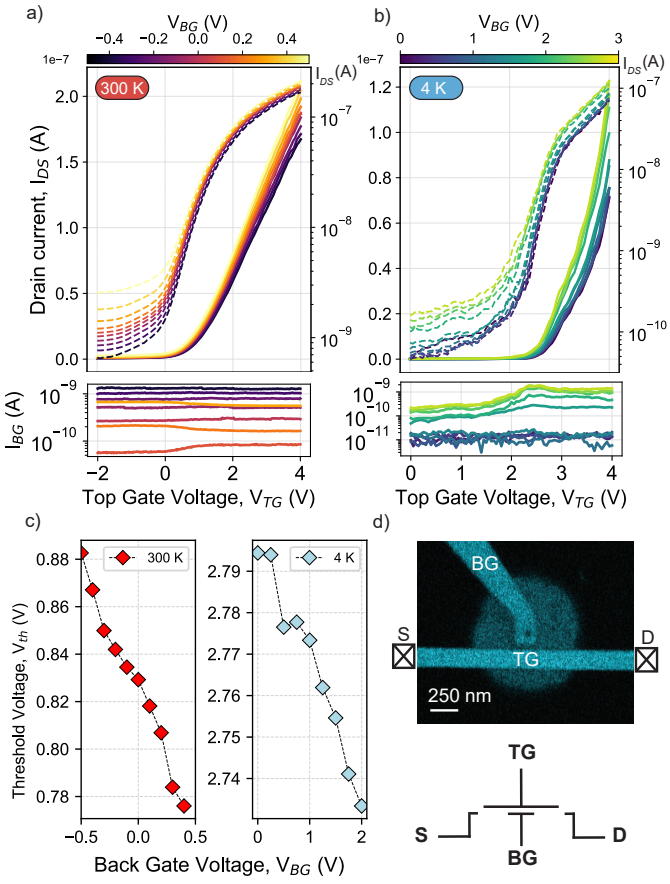

Fig. 8. Electrical characterization of a nanomole-Si FDSOI FET with 10 nm of Al_2O_3 as the top oxide, 20 nm of BOX, and 18 nm thick SOI. a-b) Transfer characteristics measured at 300 K and 4 K, respectively. V_{DS}= 0.5 V. c) Threshold voltage dependence on back-gate bias. d) SEM-EDX analysis of the device, showing contact labels and a circuit schematic.

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