Quantum Dots Array on Ultra-Thin SOI Nanowires with Ferromagnetic Cobalt Barrier Gates for Enhanced Spin Qubit Control

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Abstract

In this work we propose and demonstrate the integration of ferromagnetic nanosized cobalt barrier gates in quantum dots arrays on ultra-thin fully-depleted Silicon-On-Insulator (SOI) nanowires. This innovative structure enhances both driving and addressability, while minimizing decoherence fields for electron spin qubits. Charge noise spectra show sub-$1\cdot10^{-6}$ e^2/Hz values at 1 Hz, demonstrating a low noise impact from Co-gates. Our double dot experimental data show stable quantum confinement at 10 mK and full multi-gate FET functionality. Based on calibrated magnetic simulations, we investigate and discuss the advantages of exploiting simultaneously electrical and ferromagnetic properties of gates. The record small achieved dot-magnet distance is in the range of 5 to 12 nm, with a footprint of the magnetic gates of 30x70 nm^2 on dots area, the smallest reported to date on a qubit structure, with a Rabi frequency of 282 MHz and qubit addressability of 1.069 GHz. This novel architecture paves the way to large-scale integration of qubits arrays with unprecedented magnetic control.

Introduction

Two fundamental problems arise in large-scale integration of qubits: scalability and addressability. Linear arrays and 2D architectures have been proposed and experimentally validated with up to 6 and 9 qubits [1],[2]. However, the need for micromagnet integration and depletion gates puts stringent restrictions on layout level when scaling up, increasing the complexity of gating layers. Here we propose an architecture based on linear arrays where the ferromagnetic property of cobalt gates combines with an active DC and RF driving for qubits control, with a 2D confinement provided by ultra-thin SOI nanowires (fig. 1). This design is robust against magnets misalignment and is suitable for cross-bar addressing of qubits [3] and localized back-gate biasing for noise reduction [4].

Proof of Concept: a Double Quantum Dot

Fabrication and gates characterization - Double dot devices have been fabricated on Si nanowires (70 nm) etched on a thin SOI substrate (t_{Si}= 18 nm, t_{BOX} = 20 nm). Plunger (Pd) and barrier (Co) gates isolated with Al_2O_3 have been patterned with e-beam lithography, evaporation and lift-off, while implanted n-wells have been contacted with Ti/Pt for ohmic operation. SEM and TEM images of front and cross sections of a device are shown in fig.2, with EDX analyses. The independent electrical control of the two layers of gates at room temperature and 10 mK is reported in figs. 3, 4. The threshold voltage dependence of barrier gates on the plungers bias suggests a low inter-gate defectivity [5], validating the quality of fabrication. For large-scale integration, a self-aligned etching process could be implemented, as already reported for TiN gates [6].

Quantum confinement with ferromagnetic barrier gates- Quantum dots have been investigated with Coulomb blockade spectroscopy at mK. Periodic Coulomb diamonds and oscillations for the two dots are shown in fig. 5 and a dot capacitance of $C_{dot} \approx 27$ aF is estimated from the diamonds, giving an equivalent dot radius of $r_{dot} \approx 35$ nm in a self-capacitance disc model ($C_{dot}=8\epsilon_{eq}\epsilon_0 r_{dot}$, with $\epsilon_{eq} = (\epsilon_{Si} + \epsilon_{Al_2O_3})/2$). A lever arm of $\alpha_P \approx 0.25$ eV/V is extracted for plunger gates on 10 nm of Al_2O_3 (gate oxide), proving an excellent electrostatic control. Current and charge noise spectra ($S_I(f)$, $S_c(f)$) for a device not annealed in forming gas were performed, they are shown in fig. 6. At 1 Hz, the extracted S_c is below $1\cdot10^{-6}$ e^2/Hz, which translates into a chemical potential noise comparable with what we measured for similar devices with Pd gates only [4], demonstrating a low noise impact from Co-gates.

Magnetic Driving and Addressability of Qubits

Micromagnetic simulations have been performed with the simulation package $mumax3$ [7], assuming a cell size of 1 nm, zero temperature and cobalt with a saturation magnetization of 1.44 MA/m and exchange stiffness of 21 pJ/m. Fig. 7 shows a cross section along the nanowire direction indicating the value of Larmor frequency (f_L), driving gradient (dB_z/dx) and the decoherence gradient (dB_x/dx). At the qubit location, the driving gradient is above 10 mT/nm, while the decoherence gradient has a zero crossing. This is beneficial in terms of qubit fidelity, since a fast-driving region coincides with a charge noise protected spot along the main displacement direction. We calculate the manipulation speed (i.e. Rabi frequency) with $f_{\mathrm{Rabi}} = \frac{\gamma_e}{h}\frac{dB_z}{dx}\delta x$, where γ_e is the electron gyromagnetic ratio (g-factor of 2), h the Planck's constant and dB_z/dx the driving gradient. An oscillation amplitude (peak-to-peak) of $\delta x = 1\,\mathrm{nm}$ has been assumed [8]. The expected dephasing rate for the qubit along the direction $i \in x, y, z$ is calculated by $\Gamma_i = \pi\sqrt{2}\frac{\gamma_e}{h}\frac{dB_x}{di}\Delta i$, where we assume $\Delta x = 50\,\mathrm{pm}$ and $\Delta y,\ \Delta z = 5$ pm. The dephasing time is computed by $T_2^* = 1/(\Gamma_x + \Gamma_y + \Gamma_z)$. Due to magnetic shape anisotropy, an external magnetic field B_{ext} has to be applied to magnetize the magnetic barrier gates along x. Their magnetization pattern at varying B_{ext} and at $z = 55\,\mathrm{nm}$ is shown in fig. 8, indicating that uniform magnetization is reached above $B_{\mathrm{ext}} = 0.5\,\mathrm{T}$. In fig. 9 we plot the influence of B_{ext} on addressability (difference between qubit frequencies) , f_{Rabi} and T_2^*. In Table 1, we report the most relevant metrics taken at the foreseen qubit position with B_{ext}=1 T, and compare them with recent works. We see that f_{Rabi} and single qubit addressability are greatly enhanced with respect to current designs, with the additional advantage of the magnets not adding on the device footprint.

Summary and Perspectives

We propose an innovative architecture for arrays of spin qubits with ferromagnetic cobalt barrier gates for spin control. A Si nanowire double dot device with magnet-to-dot distance of 9 nm has been fabricated and characterized, as a validation propotype for larger arrays. Coulomb spectroscopy with low charge noise is reported and magnetic simulations predict significant improvements of the qubits metrics, with a Rabi frequency of 282 MHz and 1.069 GHz of addressability. A detailed characterization of qubits in intrinsic silicon nanowires is in progress to compare with the state-of-the art technologies.

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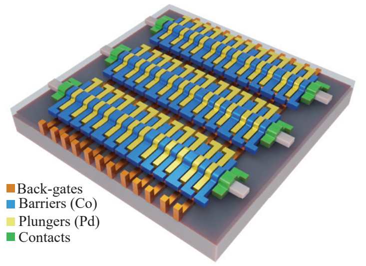


Figure 1: Proposed qubit array architecture based on Ultra-thin body SOI nanowires with magnetic gates.

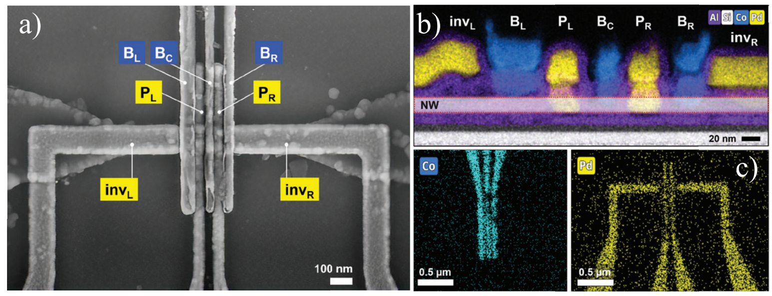


Figure 2: a) SEM image of the fabricated device. The left Co gate (60 nm wide) is 20 nm wider than the right one for the tuning of qubits addressability. b) TEM cross section of the device with EDX analysis. The thickness of the nanowire and the BOX are 18 nm and 20 nm for an optimal electrostatic control. c) EDX-SEM analysis of the gated structure.

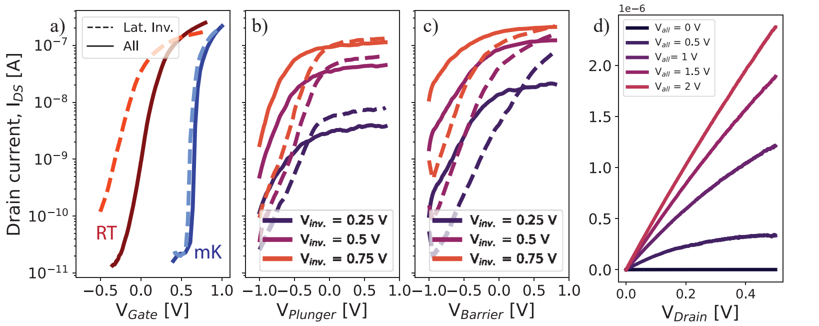


Figure 3: Pd and Co gates control at room temperature. a) I_{DS}-V_G for all gates and lateral inversion gates only. b,c) I_{DS}-V_G for plunger and barrier gates. V_{inv} denotes the voltage applied to all gates not included in the linear sweep, solid lines are for left gates, dotted lines for right gates. d) I_{DS}- V_{DS} for different bias applied to all gates.

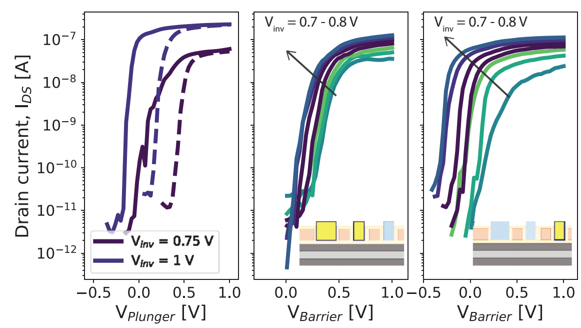
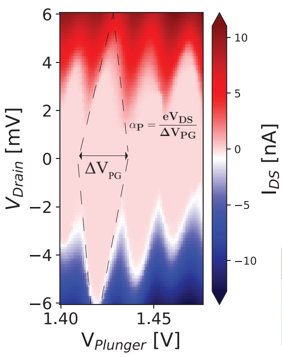
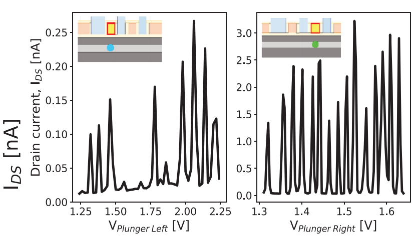


Figure 4: Gates control at mK showing the V_{th} dependence of barriers on plungers polarization. V_{inv} denotes the bias applied to all gates not included in the linear sweep.





DOT	Bar. L	Bar. Cent.	Bar. R	Pl. Left	Pl. R	Inv. L	Inv. R	V_{DS}
Left	475 mV	475 mV	400 mV	2 V	:	2.5 V	2 V	3 mV
Right	1 V	1.75 V	1.75 V	:	2 V	1.75 V	1.75 V	500 µV

Figure 5: Basic Coulomb spectroscopy at 10 mK for the left and right dot (with grounded Source). The biases applied to gates for the dots formation are listed in the table.

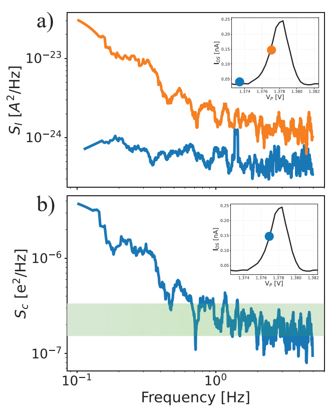


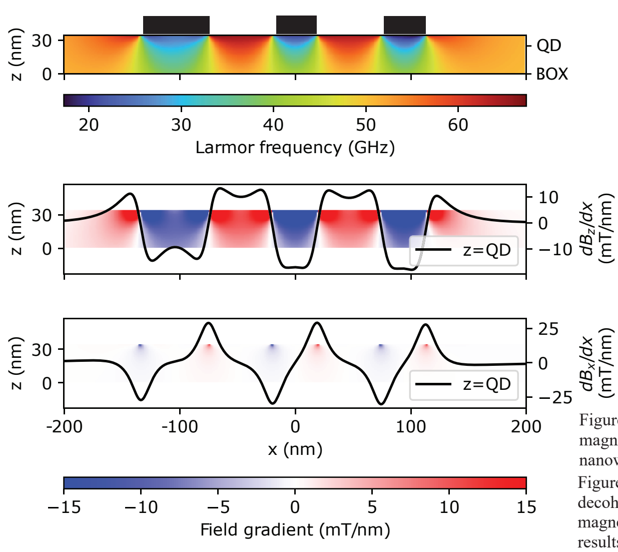
Figure 6: a) Not normalized power spectral density of current noise at the points of maximum and minimum sensitivity for one of the dots. b) Estimated charge noise computed with Eq. 1 from a $S_I(f)$ measured at the maximum transconductance (g_m) for 10 minutes at 10 mK. The device under test does not have a thermal gate oxide and was not annealed in forming gas. The noise at 1Hz compares with values reported for Pd gates with the same conditions.

Equation 1:

$$\mathbf{S_C(f)} = \alpha_{\mathbf{PG}}^2 \left|\frac{\delta \mathbf{I_{DS}}}{\delta \mathbf{V_{PG}}}\right|^{-2} \left(\frac{\mathbf{e}}{\mathbf{E_c}}\right)^2 \mathbf{S_I(f)}$$

where $g_m = \delta I/\delta V_{PG} = 114$ nS,

$E_C = 6$ meV, $\alpha_{PG} = 0.25$ eV/V



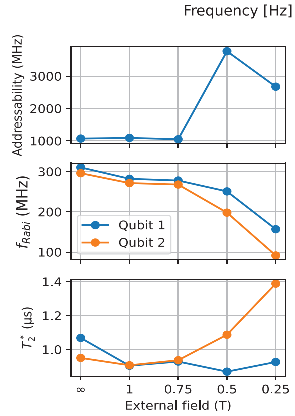


Figure 7: Simulated Larmor frequency, driving magnetic gradient and decoherence gradient along the nanowire.

Figure 9: Estimated addressability, Rabi frequency and decoherence time for the two qubits. For $B_{ext} < 0.75$ T, magnetization inhomogeneity may compromise the results.

Authors	f_{Rabi} [MHz]	Addressability [MHz]	Magnet footprint [nm²]	Dot-magnet distance [nm]	Confinement type
This work ■ ✕	282	1069	Embedded in gate metal	5-12 (gate oxide thickness)	2D
Iizuka et al. [9] ■	569	NA	30x30	15	2D
Stuyck et al. [10] ■	7	140	1000x12000 ●	120	1D
Nakamura et al. [11] ■	40	504 ▲	1600x4000 ●	150	1D
Philips et al. [1] ■ ✕	5	300	2000x8000 ●	120	1D
Yoneda et al. [12] ■ ✕	43	1290 ▲	1000x12000 ●	145	1D

■ Simulation work ✕ Magnets fabrication ● Magnets above gating structure ▲ Assuming a RMS displacement of 1 nm

Table 1: Comparison between this and other works of the main figure of merits of qubits obtained from simulations and design. The minimization of the magnet-to-dot distance is crucial for the improvement of the metrics. An experimental benchmarking will be needed to reliably compare these values.

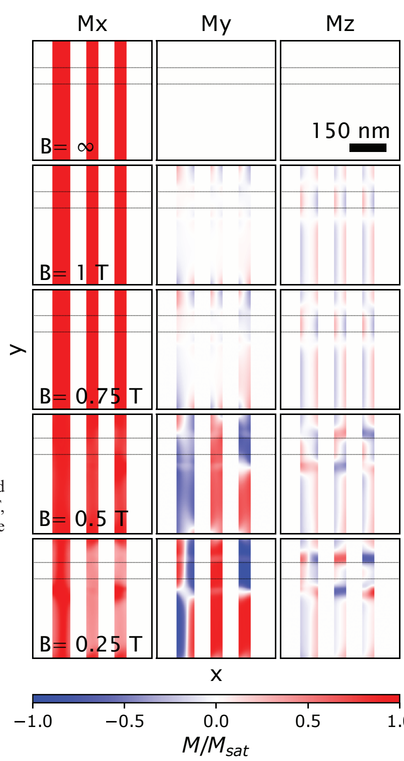


Figure 8: Simulated magnetization of cobalt gates normalized by the saturation magnetization.

References: [1] S. G. Philips, Nature, 2022, pp. 919-924. [2] P.A. Mortemousque, Nat. Nanotechnol. 16, 2021, pp. 296-301. [3] R. Li, Science Advances 4.7, 2018, pp. eaar3960. [4] F. Bersano, ESSCIRC, 2022, pp. 49-52. [5] H. Niebojewski, VLSI, 2022, pp. 415-416. [6] S. Geyer, Applied Physics Letters, 2021, 118.10, pp. 104004. [7] A. Vansteenkiste, AIP advances, 2014, 4(10), pp. 107133. [8] J.D. Teske, Physical Review B, 2023, 107.3; pp. 035302. [9] S. Iizuka, VLSI, 2021, pp. 1-2. [10] D. Stuyck, Applied Physics Letters, 2021, 119.9, p.094001. [11] S. Nakamura, Journal of Applied Physics, 2022, 132.22, p.224301. [12] J. Yoneda, Applied Physics Express, 8.8, p. 084401.