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ABSTRACT

Fast feedback from cryogenic electrical characterization measurements is key for the development of scalable quantum computing technology. At room temperature, high-throughput device testing is accomplished with a probe-based solution, where electrical probes are repeatedly positioned onto devices for acquiring statistical data. In this work, we present a probe station that can be operated from room temperature down to below 2 K. Its small size makes it compatible with standard cryogenic measurement setups with a magnet. A large variety of electronic devices can be tested. Here, we demonstrate the performance of the prober by characterizing silicon fin field-effect transistors as a host for quantum dot spin qubits. Such a tool can massively accelerate the design–fabrication–measurement cycle and provide important feedback for process optimization toward building scalable quantum circuits.

I. INTRODUCTION

The successful development of solid-state quantum hardware, such as semiconductor- or superconductor-based qubits,[1–10] requires a close interplay between device design, fabrication, and measurement. Since these structures must typically be operated in a cryogenic environment, high-throughput device testing at low temperatures (LTs) is essential to accelerate the design–fabrication–measurement cycle. However, it often takes several days to obtain characterization data from cryogenic measurements when performed on just a few wire-bonded devices, and one cooldown does not provide a statistically meaningful sample size. Additionally, devices sensitive to electrostatic discharge can be damaged during wire bonding. A non-invasive solution for high-volume cryogenic testing is to adapt conventional room temperature (RT) wafer-scale probing to LTs. Indeed, the first cryogenic 300 mm wafer prober built to guide the industrial development of quantum devices has recently been released.[11] While this probe system operates at measurement temperatures below 2 K, it may not be suitable for academic research and small-scale prototyping due to its high purchase and operational costs and limited degree of flexibility. For instance, the integration of a magnet is challenging for such large wafer sizes but would significantly strengthen the characterization toolbox. Other smaller size, commercially available systems are often based on helium-flow cryostats and, thus, suffer from device temperatures well above 4 K or a small number of probes.

We present here the setup and operation of a cryogenic probe station allowing devices to be characterized at temperatures below 2 K. It is designed for 2×2 cm^2 chips, or wafers with diameter of < 30 mm, that are moved with respect to a multi-contact probe card using closed-loop piezo-based positioners. This prober is compact enough to fit inside a standard cryogenic magnet system and is compatible with both direct-current (dc) and radio-frequency (rf) signals, thereby making it a versatile tool perfectly suited for research and prototyping. To showcase the benefit of this probe station for accelerating the design–fabrication–measurement cycle of cryogenic electronic devices, we characterize almost 50 silicon (Si) fin field-effect transistors (FinFETs) within one cooldown.

At LTs, these FinFETs host quantum dots (QDs)[12–14] such that we can obtain statistics on both transistor and QD properties.

Spin qubits in Si-based QDs[1,15–17] rank among the prime candidates for implementing large-scale quantum processors since single- and two-qubit gate fidelities exceed the fault-tolerance threshold[3,4,6] and their similarities with respect to conventional transistors allow advanced industrial manufacturing processes to be exploited.[18–20] To take full advantage of the industry's expertise to drive spin qubit development, cryogenic device testing must keep pace.

II. DESCRIPTION OF THE PROBE STATION

The main idea of RT device probing on chip- or wafer-scale is to position probe needles in contact with the bond pads of a device, to run the measurements, and to repeat this procedure in an automated way for all devices to be tested. These needles can be assembled into an array on a probe card, which, therefore, serves as a tailored interface between the measurement hardware and the device. For aligning the probe needles, a camera is used for imaging. We adopt the same principle at LT, but without imaging.

A. Design of the cryo-prober

Photographs of our cryo-prober are presented in Figs. 1(a)–1(c). The sample holder is mounted on top of an xyz piezo-based positioning unit, enabling a precise motion of the chip relative to the needles of a multi-contact wedge probe manufactured by GGB Industries. The housing of the prober is made of non-magnetic aluminum and can either be placed under a microscope at room temperature or attached via its top plate to the 1 K-pot sample mount of a variable temperature insert (VTI). A major advantage of the prober's compact design is that it can be used with cryostats readily available in academic research labs. The horizontal motion in the x- and y-directions is achieved using two attocube ANPx341/RES/LT closed-loop nanopositioners with a 20 mm travel range, which defines an upper limit for the chip area that can be tested. In addition, an attocube ANPz102/RES/LT drive with a 5 mm travel range is used for movements in the z-direction. The ANPz102 has a maximum load of 2 N, which is sufficient to push the chip into contact with the spring-loaded beryllium copper probe tips at cryogenic temperatures. This xyz-unit can be complemented by an attocube ANR101/RES/LT rotator. However, using sample holders with precisely machined cavities that host the chips, this degree of freedom was not required and, thus, was replaced by a spacer [Fig. 1(c)]. All the positioners are compatible with both mK-temperatures and large magnetic fields. The chip's coordinates are monitored using the integrated resistive encoder of the drives, which, however, is temperature-sensitive such that readout changes during cooldown or due to local heating of the resistor during the slip–stick movement of the positioners.

We measure square-shaped chips with an edge length of 2 cm and an area of 1.5×1.5 cm^2 occupied by 192 devices. The sample holder is made of either electrically conductive copper or an insulating ceramic. The latter is shown in Figs. 1(a)–1(c) and allows us to insulate the devices from the piezo positioners at RT, where the intrinsic-Si substrate is still slightly conductive. At LT, the substrate's residual conductivity freezes out and a copper sample holder is used, thermally anchored to the VTI's 1 K-pot, where the temperature T is measured.

The probe card used is a compact (max. length 44 mm and max. width 30 mm) multi-contact wedge with ten dc needles that are arranged to match the devices' bond pad layout [Fig. 1(d)]. In addition to the dc probes, such a wedge can be equipped with probes specifically designed for rf-testing.

B. Operation of the cryo-prober

We run the cryo-prober with a VTI and without optical access to the cold sample. Since the piezo's position readout depends on temperature and since, in addition, the materials contract during cooldown, the following procedure is applied to locate devices at LT: first, we determine the z-contact height z_{contact} by cooling

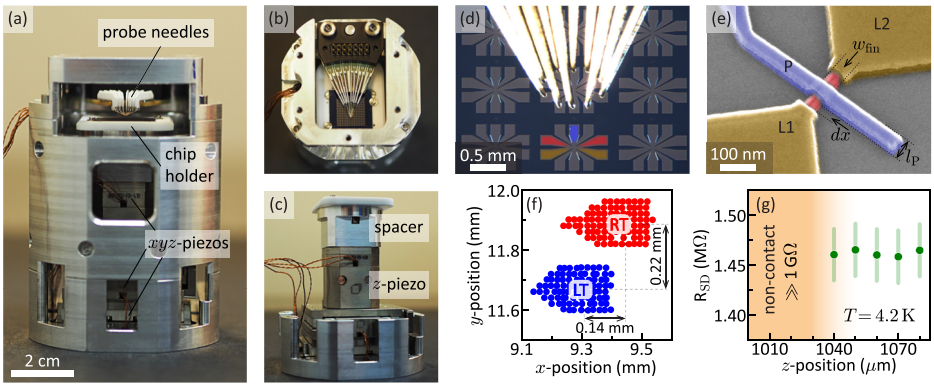

FIG. 1. Cryogenic prober setup and devices under test. Side-view [(a) and (c)] and top-view (b) photographs of the prober that consists of an xyz piezo-based positioning unit, a holder for 2 × 2 cm^2 chips, and a multi-contact wedge probe card. In (c), the housing was partially removed in order to show the z-piezo. (d) Microscope image of the probe tips with a radius of curvature of ~25 μm contacting the 150 × 150 μm^2 bond pads of a test device structure. (e) False-color scanning electron microscope image of a FinFET QD device showing the two lead gates L1 and L2 (yellow) and the plunger gate P (blue) wrapped around the Si fin (red). The five terminals required to contact such a device are highlighted in (d) using the same color code. (f) xy-marker scan, where the red and blue points indicate a current flow between two adjacent needles exceeding 0.1 nA. (g) Source-to-drain channel resistance as a function of the chip's z-position. The error bars correspond to 1σ.

down a 2×2 cm^2 Si chip with a metal (150 nm tungsten) surface coating. During cooldown, the probe is centered in the x- and y-directions over the chip and parked at the largest possible z-distance of ~1.5 mm. With a small voltage applied to one needle, the cold chip is moved up in the z-direction until this voltage is also measured on the other needles, indicating that all needles are in contact with the metal layer. Knowing z_{contact}, the differences Δx and Δy between the room and low temperature (x, y)-coordinates are characterized using a marker structure on the chips to be tested. This marker can, for example, be the bond pads of the devices, with all pads shorted together [Fig. 1(d)] or a malfunctioning device with leakage between two terminals. The latter approach is applied in Fig. 1(f), where a spatial map of the current between two probe tips, which are at slightly different voltages, is presented at RT and at $T = 4.2$ K. From these measurements, we extract $\Delta x \simeq 140$ μm and $\Delta y \simeq 220$ μm and, hence, have knowledge of the cold device coordinates as the warm ones are known. From cooldown to cooldown z_{contact}, Δx and Δy all vary by about ± 20 μm. Figure 1(g) shows the source-to-drain resistance R_{SD} of a FinFET device (discussed later) at LTs as a function of the chip's z-position: once z_{contact} is reached, R_{SD} is independent of z and we, therefore, typically work at $z = z_{\text{contact}} + \delta z$ with $\delta z \simeq 30$ μm. When the device approach is automated for chip-scale testing, one needs to consider that the heat dissipated during the piezo's slip–stick motion can alter the sensor resistance and, hence, the position readout. This issue can be counteracted by achieving a good thermal anchoring of the positioners and by dividing the movement into coarse and fine steps interleaved by a delay for thermalization. Another issue can arise from the positioner axes not being perfectly orthogonal lines, meaning that, for example, a step in x also results in a small change in y. For 150×150 μm^2 bond pads and well-thermalized positioners, an automated device approach was achieved in this work. We note that optical access to the cold sample would make the above-described techniques to characterize z_{contact}, Δx, and Δy obsolete. Illuminating the chip with light, however, may alter the devices' charge noise environment.[21,22]

III. PROBING OF Si FINFET DEVICES

We use this probe station to characterize a large number of Si FinFETs at both RT and LT. As shown in the scanning electron microscope image of Fig. 1(e), the devices under test have one plunger (P) and two lead gates (L1 and L2); the p-type source and drain regions are made of platinum silicide (PtSi). These devices are designed to create accumulation-mode hole QDs; further details are given elsewhere.[13,14] Recently, we used similar devices to demonstrate single-qubit gate operations above 4 K[23] and two-qubit logic with anisotropic exchange[24] for holes in FinFETs. The chip's 192 devices are arranged on a 12-by-16 grid, in which the fin width w_{fin}, plunger gate length l_P, and gate spacing dx [Fig. 1(e)] are varied (see the supplementary material S1 for a map of the chip with device dimensions). Unfortunately, the sample space diameter of the VTI available to us restricted the travel range of the x- and y-positioners such that only 60 devices could be approached. For testing of these five-terminal devices, five out of ten needles land on a bond pad [Fig. 1(d)] and the others on an ~100 nm-thick silicon oxide layer. We test the devices by applying dc voltages and measuring the current response using a low-noise voltage source (BasPI SP927) complemented by a current monitoring box (BasPI SP1046). If more gain variability is required for current measurements, current-to-voltage amplifiers (BasPI SP983c) are utilized. All voltage signals are digitized with a National Instruments USB-6363 data acquisition card.

A. Comparison of room and low temperature measurements

First, in Fig. 2, we compare transistor characteristics at RT and $T = 4.2$ K. Out of the 60 accessible devices, 48 (44) worked fine at LT (RT) (four were damaged during cryogenic testing requiring larger applied voltages). We record the source-to-drain current I_{SD} while monitoring the gate leakage currents. If one of the latter exceeds a limit, the ongoing measurement is aborted and the tool automatically moves to the next device. In Fig. 2(a), the plunger gate

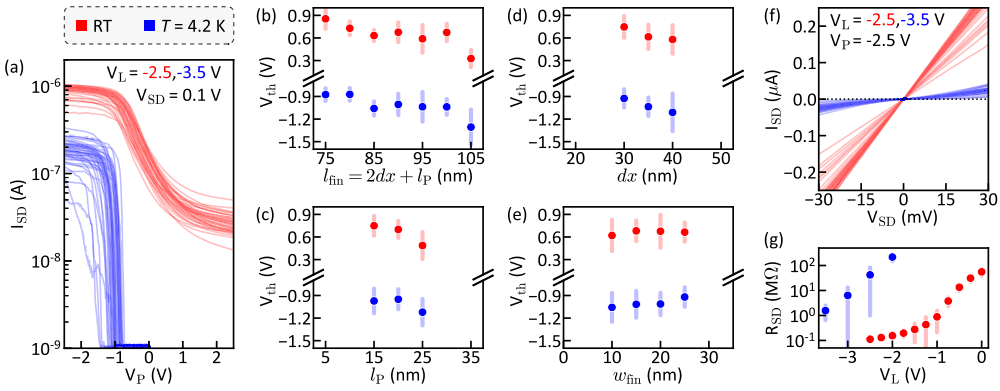

FIG. 2. Transistor autoprobing at RT (red, 44 devices) and $T = 4.2$ K (blue, 48 devices). (a) Transistor turn-on curves in the high-bias regime. For the logarithmic current scale, the zero-current flow from source to drain corresponds to 1 nA. (b)–(e) Plunger gate threshold voltage dependence on the device dimensions. (f) I_{SD} vs V_{SD} curves measured in the transistor on-state, i.e., $|V_P| > |V_{th}|$. (g) Effect of lead gate voltage on channel resistance. Plotted are the mean values with 1σ error bars from all measured devices.

voltage V_P is swept for a source–drain voltage V_{SD} of 100 mV and a lead gate voltage V_L that is sufficiently above the threshold (see the supplementary material S2 for lead gate sweeps). While, at LTs, the channel can be switched off completely, at RT, a finite current flows in the transistor's off-state due to conduction via the Si substrate. Moreover, the switching to the on-state is much steeper at 4.2 K and occurs for a threshold voltage V_{th} of -1.01 ± 0.17 V (averaged over all devices) in contrast to $+0.64 \pm 0.18$ V at RT. The dependence of V_{th} on the device dimensions is presented in Figs. 2(b)–2(e). These curves highlight how the probing of a statistically meaningful sample size enables trends to be identified. For instance, the threshold voltage decreases (increases) when the transistor channel length (width) is increased. Even though the V_{th}-values are offset, the absolute change is almost the same at LTs and RT. The plunger gate sweeps also reveal that the on-state current of the transistors is reduced at 4.2 K, which is confirmed by the I_{SD}–V_{SD} curves presented in Fig. 2(f). While they are linear at RT, they are non-linear at LTs, where the presence of the Schottky barrier at the PtSi–Si junction is noticed more.[13] As shown in Fig. 2(g), R_{SD} depends strongly on V_L. While the resistance saturates at ~100 kΩ for RT, no saturation effect is observed even at $V_L = -3.5$ V for $T = 4.2$ K. More negative lead gate voltages were not applied in order to avoid damaging the devices.

B. Quantum dot characterization

We next turn to the characterization of QDs, which requires cryogenic temperatures. An example of a plunger gate sweep recorded at $T = 4.2$ K with $V_{SD} = 1$ mV and $V_L = -3.5$ V is given in Fig. 3(a) (see the supplementary material S3 for the same measurement repeated on all other devices). Here, a series of Coulomb resonances demonstrates single-hole tunneling via a QD that has formed beneath the plunger gate. Between the peaks, the device is in Coulomb blockade; that is, the number of holes residing on the QD is fixed.[12] Eventually, the plunger gate's fringe fields lower the tunnel barriers such that, for $V_P \lesssim -1.3$ V, a conducting channel opens.[13] The closing of the Coulomb diamonds in Fig. 3(c) indicates the formation of a single QD below the plunger gate with charging energies up to ≃20 meV. We examine the actual device cooling by means of Coulomb blockade thermometry: in the weak-coupling limit $\hbar\Gamma \ll k_B T$ and for small source–drain voltages, the current resonances are thermally broadened, thus allowing us to experimentally determine the hole temperature T_h. Here, $\hbar$ denotes the reduced Planck constant, k_B is the Boltzmann constant, and Γ is the tunnel coupling between the QD and reservoir states. In Figs. 3(b) and 3(a), a high-resolution zoom-in on the first observable Coulomb peak recorded at $V_{SD} \simeq 0.1$ mV for $T = 4.2$ K and $T = 1.8$ K is shown. By fitting the function[25] $I_1 \cosh^{-2}[\alpha(V_{P,c} - V_P)/(2k_B T_h)] + I_0$ to the data, a T_h of 4.5 ± 0.3 and 2.3 ± 0.4 K is extracted. Here, $V_{P,c}$ denotes the peak center position and $\alpha \simeq 0.32$ eV/V is the plunger gate lever arm that is obtained from the Coulomb diamond plotted in Fig. 3(c). The hole temperatures are slightly above the ones measured with the 1 K-pot thermometer, indicating an insufficient thermal anchoring of the chip or the VTI's dc lines. Both can be improved, and device temperatures down to ≃1.5 K are within reach.

Finally, we remark that the cryo-prober allows currents to be measured with the same low noise level as achieved when characterizing wire-bonded devices; Fig. 3 confirms that currents <100 fA are detectable.

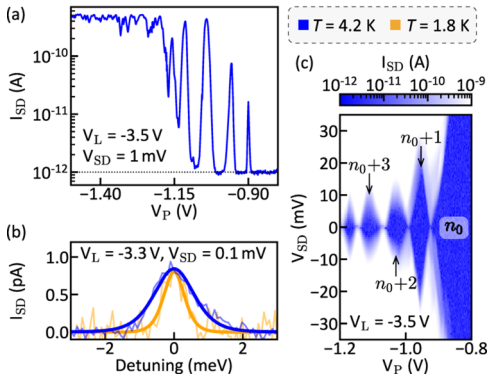

FIG. 3. QD measurements at 4.2 K (blue) and at 1.8 K (orange). (a) Plunger gate sweep in the low bias regime with well-pronounced Coulomb blockade oscillations. (b) Extraction of the hole temperature by fitting the first observable Coulomb blockade peak. A hole temperature of 4.5 ± 0.3 and 2.3 ± 0.4 K is found, respectively. (c) Charge stability diagram revealing the formation of a single QD. The data presented in this figure are measured on a device with $w_{fin} \sim 15$ nm, $l_P \sim 15$ nm, and $dx \sim 35$ nm.

IV. CONCLUSIONS

In conclusion, we designed, built, and operated a cryogenic probe station enabling automated probing of electronic devices below 2 K, a device temperature not reached by any other compact, commercially available probe system. The instrument's value for accelerating the design–fabrication–measurement cycle is demonstrated by testing almost 50 Si FinFET devices at both room and low temperature. Probing of a statistically significant number of devices allows us to reliably extract transistor and QD properties and identify trends and patterns in the data. Besides high-throughput device testing, the prober can be utilized to search for the highest quality devices for subsequent dilution refrigerator experiments. The prober's degree of automation can be further enhanced by (i) implementing optical access to the cold sample, enabling device localization via image pattern recognition, and (ii) using machine learning for completely automatic tuning of quantum devices.[26–28] Optical access also allows for the implementation of optical-based characterization techniques. Furthermore, the prober can be upgraded with a magnet and rf probes such that not only transistor and QD characteristics but also statistics on qubit parameters can be obtained. This functionality is especially useful for Si QD spin qubits since recent work has shown that these can be operated at temperatures of up to 5 K.[23,29–31]

SUPPLEMENTARY MATERIAL

See the supplementary material for a map of the chip with device dimensions, lead gate sweeps at RT, and low-bias plunger gate sweeps at 4.2 K performed on all devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Mathieu de Kruijf: Conceptualization (equal); Data curation (lead); Formal analysis (lead); Investigation (lead); Methodology (lead); Software (lead); Visualization (equal); Writing – original draft (lead); Writing – review & editing (lead). **Simon Geyer**: Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Software (supporting); Writing – review & editing (supporting). **Toni Berger**: Conceptualization (supporting); Investigation (supporting); Methodology (supporting); Software (supporting); Writing – review & editing (supporting). **Matthias Mergenthaler**: Conceptualization (supporting); Methodology (supporting); Writing – review & editing (supporting). **Floris Braakman**: Conceptualization (supporting); Methodology (supporting); Resources (supporting); Writing – review & editing (supporting). **Richard J. Warburton**: Conceptualization (supporting); Funding acquisition (equal); Investigation (supporting); Methodology (supporting); Project administration (equal); Resources (equal); Supervision (equal); Writing – review & editing (supporting). **Andreas V. Kuhlmann**: Conceptualization (lead); Data curation (lead); Formal analysis (lead); Funding acquisition (lead); Investigation (lead); Methodology (lead); Project administration (lead); Resources (lead); Software (lead); Supervision (lead); Validation (lead); Visualization (lead); Writing – original draft (lead); Writing – review & editing (lead).

DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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